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Advances in SiC Materials, Processes, and Devices Unveiled

(See MRS Proceedings Volume 742)

Symposium K is the second in a series of SiC symposia at the MRS Fall Meeting. Since the last meeting in 2000, advances in SiC materials, processing, and device design have resulted in implementation of SiC-based electronic systems and offer great promise in high-voltage, high-temperature, high frequency applications. Presenters focused on new developments in the basic science of SiC materials as well as rapidly maturing device technologies. The challenges in this field include understanding and decreasing defect densities in bulk SiC crystals, controlling morphology and residual impurities in epilayers, optimization of implant activation and oxide-SiC interfaces, and developing novel device structures.

Topics of particular interest were in the area of bulk SiC growth (including large-diameter crystals), modeling, characterization, homo- and heteroepitaxial growth (e.g., doping control, morphology development, and carrier lifetimes), advances in ion implantation, improved ohmic and rectifying contacts, surfaces and interfaces, oxidation, and alternative dielectric materials and devices (including high-voltage, high-temperature, high-frequency sensors and system level benefits).

Symposium Support: ARL, NASA Glenn Research Ctr., and ONR.

Report for ONR
Material Research Society Symposium K
Silicon Carbide: Materials, Processing, and Devices
Boston, MA., Dec. 2-4, 2002

Chairmen:
Stephen E. Saddow, Nelson Saks, David J. Larkin, Adolf Schoner, and Marek Skowronski

General Summary:

There were nearly 100 papers presented at the symposium with 16 invited talks, 24 Oral talks and 45 Poster presentations. Overall, the presented papers were well attended and generated very useful discussions, thereby contributing greatly to the overall success of the symposium. One of the conference poster papers entitled Confinement of Screw Dislocations to Predetermined Lateral Positions in (0001) 4H-SiC Epilayers using Homoepitaxial Web Growth , presented by Dr. Philip Neudeck and co-workers won a best poster of the conference award.

The research presented at this symposium represented the latest activities in SiC research and development since the International Conference on SiC and Related Materials (ICSCRM) which was held in Tsukuba, Japan in October 2001. The field of SiC is rapidly maturing and the symposium reflected this maturity, with many industrial talks providing good insight into what industry perceives to be the key issues and technological challenges to overcome so that SiC can more rapidly enter the marketplace. A proceedings volume from this symposium is being prepared.

We gratefully acknowledge the financial support provided by the Office of Naval Research, the Army Research Laboratory, the NASA-Glenn Research Center, and the Materials Research Society.

Highlights of presentations:

Several papers at the meeting presented significant advances in epitaxial growth, materials characterization, processing, and device performance. The invited paper by Ulrich Starke on the Reconstruction and Epitaxial Adlayers on SiC Surfaces: Structural Significance for Technological Applications, provided insight into SiC epitaxial growth and the influence of the starting surface on oxide growth. Another invited talk, by Hiroyuki Nagasawa, presented the latest work on heteroepitaxy of 3C-SiC on Si substrates involving on growing 3C-SiC on (001) undulant Si. This work describes the impressive ability to form thick (~200 um) free-standing layers of cubic SiC that can then be used for further materials growth or device processing. Indeed the invited paper by Prof s W.J. Choyke and R.P. Devaty described some very interesting recent results in the characterization of SiC, including optical characterization of the free-standing 3C-SiC layers grown on the undulant Si substrates. A paper entitled Recent Results on Defect Centers in SiC Poly-types, by Gerhard Pensl presented an extensive discussion regarding proper determination of the Hall Scattering coefficient in SiC which showed good correlation between Hall free-carrier concentration, CV and SIMS measurement of doping concentration.

One of the recent challenges for SiC is the identification of stacking faults that are nucleated in heavily-doped 4H-SiC bi-polar devices. This is of critical concern to the community since 4H-SiC is the leading candidate (compared to 6H-SiC) for high-power switching devices due to its high, nearly-isotropic electron mobility. Two excellent papers were presented by the NRL group on this topic: Dependence of Stacking Fault Growth Dynamics on Current Through SiC PIN Diodes, by R.E. Stahlbush and co-workers. and Extended Defects in 4H SiC PIN Diodes, by M.E. Twigg and co-workers.

Another area of keen interest in SiC technology is the role that hydrogen plays in altering the doping density through the formation of complexes. This is especially a concern in p-type material where hydrogen can passivate acceptors, thus lowering the net hole concentration. A very nice talk was given by Dr. Yaroslav Koshka entitled Optically Enhanced Interaction of Hydrogen With Defects in SiC which outlined a detailed study of the effects of hydrogen on the PL spectra of SiC samples that were hydrogenated using a hydrogen plasma source. The results were correlated with SIMS profiles and gave consistent results with one major exception — CV measurements were not reported which would be the final proof that hydrogen passivation can be removed with thermal annealing.

In the processing session, an invited talk was presented by Marina Mynbaeva on Porous Silicon Carbide: Prospective Applications . This work presented a review of research on porous SiC at Ioffe Institute (St. Petersburg, Russia) and also on new work on doping by out-diffusion. Results pointing towards the possible use of porous SiC as a compliant substrate were also presented. The ONR DURINT program was acknowledged during this presentation as the source for much of the progress in this field in recent years.

In the device arena, several exciting industrial talks were presented which outlined progress being made to insert SiC devices into commercial and military systems. The three most notable talks were given by Infineon and Cree, and covered the range from unipolar, bipolar and RF/High power switching devices. Clearly SiC device technology is rapidly maturing, and results that represent significant advances from previous work was reported. The three papers of discussing these advances are: System Design Considerations for Optimizing the Benefit by Unipolar SiC Power Devices, by Roland Rupp and co-workers, PiN Rectifiers and Bipolar Switches in 4H-SiC, by Ranbir Singh and co-workers, and SiC Bipolar Junction Transistors for High Power Switching and RF Applications, by Anant Agarwal and co-workers.

Regarding MOS devices on SiC, a review of current state-or-the-art oxidation was presented by Len Feldman of Vanderbilt Univ. This work presented current understanding of nitridation techniques, including anneals in NO and other nitrogen species, for reducing the high interface trap densities in MOS oxides on 4H-SiC. Lisa Porter presented an invited talk on the nano-scale buildup of interfacial carbon after oxidation of the SiC surface. H. Yano of Kyoto Univ. gave an invited talk on interface properties for different SiC interfaces showing the potential advantages of the <11-20> and <03-38> orientations. A. Hoff of the Univ. of S. FL presented a talk on very low-temperature oxidation of SiC using a downstream afterglow of an oxygen plasma. Finally, Ruby Ghosh of Mich. State gave an invited talk on the effects of high temperatures and hydrogen, oxygen, and vacuum ambients on interface traps in MOS devices with platinum gates.

This system appears to provide the first *reproducible* technique for passivation and de-passivation of traps at the SiC/SiO_2 interface.

SYMPOSIUM K

Silicon Carbide—Materials, Processing, and Devices

December 2 – 4, 2002

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* Invited paper

SESSION K1: EPITAXIAL GROWTH
Chairs: David J. Larkin and Tsunenobu Kimoto
Monday Afternoon, December 2, 2002
Room 206 (Hynes)

1:30 PM *K1.1
EPITAXIAL GROWTH AND CHARACTERIZATION OF 4H-SiC(11$\bar{2}$0) AND (03$\bar{3}$8). Tsunenobu Kimoto, Shun-ichi Nakamura, Keiko Fujihira, Kouichi Hashimoto, Katsunori Danno, Yuuki Negoro, and Hiroyuki Matsunami, Department of Electronic Science and Engineering, Kyoto University, Kyoto, JAPAN.

4H-SiC(0001) wafers with several-degree off-angles have exclusively been employed for SiC homoepitaxy and device development, owing to their availability. Major drawbacks of the (0001) face include threading micropipes (super screw dislocations), which severely affect blocking performance of high-voltage SiC devices, and unacceptably low channel mobility of MOSFETs. The authors have proposed novel crystal faces, 4H-SiC(11$\bar{2}$0) and (03$\bar{3}$8), both of which exhibit superior MOS interface properties, compared to the conventional (0001). In this paper, epitaxial growth, defect reduction, physical properties, and impurity doping of 4H-SiC(11$\bar{2}$0) and (03$\bar{3}$8) are reviewed. 4H-SiC(11$\bar{2}$0), equivalent to (110) in the cubic structure, is parallel to the c-axis, and naturally is micropipe-free. The reduction of stacking faults and growth of large boule crystals are challenges for 4H-SiC(11$\bar{2}$0). 4H-SiC(03$\bar{3}$8) is the face inclined by 54.7° from (0001), and is semi-equivalent to (100) in the cubic structure. Homoepitaxial growth was performed by CVD in a SiH_4-C_3H_8-H_2 system. Although the incorporation efficiency of nitrogen donor is higher on these novel faces than on (0001), a low background doping concentration of 1×10^{14} cm^{-3} (n-type) or less has been achieved by CVD growth under C-rich conditions. DLTS analyses revealed one electron trap located at E_C-0.68 eV. However, the trap concentration is sufficiently low, $1\text{-}3\times10^{12}$ cm^{-3}. Molten KOH etching at 480°C was employed to identify structural defects in crystals. Successive etching experiments (etching/microscope-observation/polishing process was repeated) on 10-110 μm-thick 4H-SiC(03$\bar{3}$8) epilayers revealed that very few (< 1 cm^{-2}) micropipes exist in 4H-SiC(03$\bar{3}$8) epilayers, while micropipes with a density of 10-50 cm^{-2} appeared when substrates were etched after polishing away epilayers. This result indicates that micropipes are dissociated or transformed in structural nature near the (03$\bar{3}$8) epilayer/substrate interface.

2:00 PM *K1.2
CHANNEL EPITAXY OF OF 3C-SiC ON Si SUBSTRATES BY CVD. S. Nishino, Y. Okui, C. Jacob† and S. Ohshima, Kyoto Institute of Technology, Department of Electronics and Information Science, Kyoto, JAPAN; †Materials Science Centre, Indian Institute of Technology, Kharagpur, INDIA.

Cubic silicon carbide has been grown epitaxially on Si substrates for many years. The heteroepitaxial growth of 3C-SiC on Si has indicated the promise of high mobility devices. However, a high density of interfacial defects (misfit dislocations, voids) as well as other defects (threading dislocations, twins, stacking faults) result in the growth of lower quality material. A suitable approach towards solving this problem is the use of selective epitaxial growth on patterned silicon substrates followed by lateral epitaxial overgrowth (LEO). LEO in GaN growth on 6H-SiC [and Sapphire has been successful. The technique has successfully been applied to grow 3C-SiC on Si [6,7]. The above work was done on Si (100) substrates. This approach prevents the propagation of threading dislocations originating from the 3C-SiC/Si interfaces. Therefore, lateral growth of a 3C-SiC layer until coalescence results in a 3C-SiC layer of low defect-density material. In this paper, we report on a promising technique of selective epitaxial growth of 3C-SiC combined with lateral epitaxial growth on patterned Si substrates to further illustrate the application of this technique to the growth on Si substrates. The use of HCl on growth influences the surface morphology]. This approach has been developed for not only reduction of defects but also decrease the influence of mask materials.

2:30 PM K1.3
MODELLING ANALYSIS OF FREE-SPREADING SUBLIMATION GROWTH OF FACETETED SiC CRYSTALS. M.V. Bogdanov, S.E. Demina, S.Yu. Karpov, A.V. Kulik, D.Kh. Ofengeim, M.S. Ramm, Soft-Impact Ltd, St. Petersburg, RUSSIA; E.N. Mokhov, A.D. Roenkov, Yu.A. Vodakov, Crystal Growth Science and Technology Lab, St. Petersburg, RUSSIA; Yu.N. Makarov, Semiconductor Technology Research Inc, Richmond, VA; H. Helava, The Fox Group Inc, Livermore, CA.

A new advanced technique for growing of free-spreading SiC bulk crystals by sublimation has recently been suggested. In this method, the growing crystal does not contact the crucible wall during the whole growth process. 6H- and 4H-SiC boules free of polycrystalline deposits along the crystal perimeter up to 35mm in diameter with the micropipe density less than 20cm^{-2} and the dislocation density about 10^2-$10^3$$cm^{-2}$ have been grown by this technique. In the best crystals, there are large areas free of micropipes and dislocations. To get better insight into the growth process, we used numerical modelling performed by the software tool "VirtualReactor". The modeling task includes simulation of global heat transfer in the inductively heated growth system, as well as species transport in the growth cell. Special attention is given to the verification of the simulations. We compared computed thermal field, growth rate and the crystal shape evolution with experimental data. The comparison showed that results of the computations agree well with experiments. To optimize the growth system design and the operating conditions, we used an approach based on the inverse modeling. This procedure utilizes the numerical optimization methods and allows obtaining the system design and operating conditions providing the optimal thermal field in the growth cell, desired crystal shape evolution and reduced elastic stresses in the crystal. Joint modeling and experimental effort allowed to grow bulk SiC crystals with reduced defect densities.

2:45 PM K1.4
EXPERIMENT AND MODELING OF THE LARGE AREA ETCHING AND GROWTH RATE OF EPITAXIAL SiC. J. Meziere, M. Pons, J-M Dedulle, E. Blanquet, CNRS Grenoble, FRANCE; L. Di Cioccio, P. Ferret, T. Billon, CEA-Grenoble, FRANCE.

The growth of thick and high quality epitaxial 4H-SiC layers, needed for high power devices requires a good control of the CVD processes. We realized such layers in an horizontal hot-wall reactor commercialized by the Epigress-Aixtron company. The numerical approach was used first to optimize its design [1]. In this paper, a chemistry model including surface deposition and etching is described and then compared to experimental data to validate the model on large-scale area growth. The complete chemistry model [2] has been reduced to few binary species like SiH_2, Si, C_2H_2, C_2H_4, CH_4, CH_3 and organo-silicon species like Si_2C, H_3SiCH_3 and $HSiCH_3$ have been added. An etching model fitted with the experimental results has been included in the surface chemistry. Three wafers of 2" were placed on the susceptor to measure the etch rate. This experiment underline that the hydrogen etching is an important phenomena for typical process conditions and that etched species contribute to deposition on the last wafer. Five wafers of 2" were placed on the susceptor to measure the growth rate profile. The results show that there is a region of 100 mm where the growth rate is uniform. The analysis of the wafers with optical microscopy reveals three zones with different morphologies. At the entrance of the susceptor (0-100 mm) the layer is polycrystalline and rich in silicon. In the next region (100-200 mm), the layer is of high quality. At the end of the susceptor, a lot of defects are observed in the layer. An excellent agreement between experimental and numerical results have been achieved when gas and surface chemistry include etching phenomena during the growth process. [1] M. Pons, J. Meziere, S. Wan Tang et al. J. Phys IV France, 1079 (2001). [2] M.D. Allendorf, R.J. Kee, J. Electrochem. Soc., 138(3), 841 (1991).

3:30 PM *K1.5
RECONSTRUCTION AND EPITAXIAL ADLAYERS ON SiC SURFACES: STRUCTURAL SIGNIFICANCE FOR TECHNOLOGICAL APPLICATIONS. Ulrich Starke, Max-Planck-Institut für Festkörperforschung, Stuttgart, GERMANY.

The structure and composition of SiC surfaces is of great importance for growth of SiC material and epitaxial deposition of oxides and metals. Most SiC applications are implemented on hexagonal surfaces, i.e. the silicon or carbon terminated bilayer truncation planes perpendicular to the c-axis. In this paper structure and composition are reviewed for different surface phases on both SiC(0001) and SiC(000$\bar{1}$), the orientations nominally terminated by silicon and carbon, respectively. The immediate relevance of the atomic surface structure for technological applications is demonstrated for examples related to single crystal growth, heterojunctions and oxidation. Surface preparation was carried out *ex situ* by hydrogen treatment or in vacuum by Si deposition and annealing. For surface characterization scanning tunneling microscopy (STM), Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and low-energy electron diffraction (LEED) crystallography were used. The chemistry of well ordered phases spans from Si rich to graphitic composition with the excess elements arranged in adlayers and/or large scale reconstruction patterns. A Si rich surface, namely the (3×3)-SiC(0001) phase, allows for step flow growth of monocrystalline homoepitaxial layers due to an extremely efficient dangling bond saturation. Si rich preparation or oxidative treatment are used for a controlled evolution of different stacking sequences on the $(\sqrt{3}\times\sqrt{3})$R30° phase on SiC(0001) and could be utilized for the development of polytype heterostructures. An epitaxially well matching silicon oxide monolayer can be prepared on both surface orientations by using a hydrogen etching or plasma treatment promising to facilitate low defect oxide films for MOS devices.

4:00 PM *K1.6
3C-SiC MONOCRYSTALS GROWN ON UNDULANT Si(001) SUBSTRATES. Hiroyuki Nagasawa, Kuniaki Yagi, Takamitsu Kawahara, Naoki Hatta, Hoya Advanced Semiconductor Technologies Co. Ltd, Tokyo, JAPAN.

In spite of its great advantages, such as isotropic electron mobility and high saturation velocity of electrons, device applications using 3C-SiC have lagged significantly behind those using hexagonal-SiC, owing to the large number of planar defects (anti-phase boundary and stacking faults) in this material. Recently, we developed a novel technique that effectively reduces planar defects in the 3C-SiC epitaxial layer by growing it on an undulant-Si substrate. This substrate has a wavy surface, consisting of a Si(001) base with countered slopes oriented in the [110] and [-1-10] directions. During initial 3C-SiC growth, the anti-phase boundaries (APBs) are eliminated on each slope of the undulant-Si by the same mechanism previously found in the case of epitaxy on slightly mis-oriented Si(001). While the 3C-SiC grows thicker, the stacking fault (SF) density also decreases through shrinkage or annihilation mechanisms. At the meeting, the reduction mechanisms of the planar defects will be discussed in detail. Then the properties of low defect 3C-SiC substrates will be discussed, based on the results of XTEM observations and the Hall effect.

4:30 PM K1.7
GROWTH OF COLUMNAR SiC ON PATTERNED Si SUBSTRATES BY CVD. Shigehiro Nishino, Yoich Okui, Yuehai Tai, and Chacko Jacob†, Kyoto Institute of Technology, Department of Electronics and Information Science, Kyoto, JAPAN. †Materials Science Centre, Indian Institute of Technology, Kharagpur, INDIA.

The heteroepitaxial growth of 3C-SiC on Si and other substrates has indicated the promise of high mobility devices and also application for MEMS. In MEMS application, a suitable approach is the use of selective epitaxial growth of Si and SiC on patterned silicon substrates.The substrates used were patterned silicon substrates prepared by depositing a SiO2 layer as the mask, followed by conventional lithographic techniques. The windows are of different shapes (square, circle, hexagonal, parallel lines). Selective growth of Si was carried out by hydrides(HCl) transport method in H2 atomosphere at around 1200°C. A columnar structure of Si was automatically produced on the patterned substrate. Si column grew on the Si windows and small sphere grew on the SiO2. An initial carbonization procedure was performed using 1 sccm propane at 1250°C for 2-3 minutes. During the growth of SiC, the flow rate of HMDS was 0.1-0.75 sccm and the flow rate of HCl, with a flow rate of 1.0 - 2.0 sccm, was used as an etchant as well as to suppress unwanted nucleation on the SiO2 mask. SiC covered small column is applicable to MEMS device. The characterization of the SiC covered Si column will be discussed.

SESSION K2: POSTER SESSION
Chair: David J. Larkin
Monday Evening, December 2, 2002
8:00 PM
Exhibition Hall D (Hynes)

K2.1
ION DOSE DEPENDENCE ON SOLID PHASE EPITAXY OF AMORPHOUS SILICON CARBIDE INDUCED BY ION IMPLANTATION. In-Tae Bae, Dept of Materials Science and Engineering, Osaka Univ, Osaka, JAPAN; Manabu Ishimaru, Yoshihiko Hirotsu, The Institute of Scientific and Industrial Research, Osaka Univ, Osaka, JAPAN.

Silicon carbide (SiC) is an important semiconductor material due to its application for electronic and optoelectronic devices. From the viewpoint of processing technology, it has been revealed that conventional diffusion-based techniques can not be applied since diffusivity of impurities in SiC is very low below 1700°C. As an alternative method, solid phase epitaxy (SPE) of ion-beam-induced amorphous SiC is an important technique. Compared with the threshold crystallization temperature of 1450°C which had been accepted generally, recent studies have shown that recrystallization of implantation-induced amorphous already occurs at a temperature as low as *char char* 800°C. This discrepancy is due to a lack of knowledge about recrystallizaion process in amorphous SiC. Particularly, no work has been performed to study the relationship between ion doses and threshold crystallization temperatures. In this work, we prepared two different specimens of amorphous SiC layers fabricated by Xe ion implantation with ion doses 10 times different each other (10^{15} and 10^{16} cm^{-2}), and annealed them at temperatures ranging from 800 to 900°C. Cross-sectional TEM images of as-implanted specimens revealed that complete amorphization occurred in both of high dose and low dose specimens with thickness of *char char*120 and *char char*80 nm, respectively. After annealing at 850°C for 1 h, low dose specimen was recrystallized completely, while high dose specimen was not recrystallized. Almost all of the part of high dose specimen remained as amorphous state with only small discrete area of recrystallization near surface. This result suggests that recrystallization threshold temperature for SPE depend on amorphous state which is not a single structure [1]. [1] M. Ishimaru, I.-T. Bae, Y. Hirotsu, S. Matsumura, K.E. Sickafus, Phys. Rev. Lett. (in press).

K2.2
RADIAL DISTRIBUTION FUNCTIONS OF AMORPHOUS SILICON CARBIDE. Manabu Ishimaru, In-Tae Bae, Yoshihiko Hirotsu, Osaka Univ, The Institute of Scientific and Industrial Research, Osaka, JAPAN.

Although extensive studies have been carried out on structural analyses of amorphous silicon carbide (a-SiC), on the fundamental nature of short-range order in a-SiC remains a topic of debate. Some researchers characterized a-SiC networks as highly chemically ordered, consisting of heteronuclear (Si-C) first nearest neighbor bonds. On the other hand, there is evidence for the formation of homonuclear bonds (Si-Si and C-C bonds) in a-SiC. We have examined amorphous structures of SiC using both transmission electron microscopy and a molecular-dynamics approach. Single crystal wafers of (0001)-oriented 6H-SiC were irradiated at room temperature with 150 keV argon (Ar^+) ions to a fluence of 10^{16} /cm^2. This ion irradiation procedure produced an a-SiC layer ~200 nm thick on the surface of the SiC wafers. The intensities of the halo pattern obtained from the amorphous layer were analyzed quantitatively using an imaging plate. Radial distribution functions revealed the existence of C-C and Si-Si bonds in the first coordination shell of a-SiC. This suggested that a-SiC possesses not only heteronuclear bonds but also homonuclear bonds. The ratio of heteronuclear to homonuclear bonds was found to change upon annealing: the peaks associated with heteronuclear bonds became more pronounced during annealing, while peaks corresponding to homonuclear bonds simultaneously decreased. Good agreement was obtained between the simulated and experimentally measured radial distribution functions. [1] M. Ishimaru, I.-T. Bae, Y. Hirotsu, S. Matsumura, K.E. Sickafus, Phys. Rev. Lett. (in press).

K2.3
MEMORY SWITCHING IN IMPLANTED HYDROGENATED AMORPHOUS SILICON CARBIDE THIN FILM DEVICES. R.G. Gateru, J.M. Shannon, S.R.P. Silva, University of Surrey, School of Electronics, Computing and Mathematics, Guildford, Surrey, UNITED KINGDOM.

Memory switching in amorphous silicon alloys has been studied for many years. Of particular interest is switching in amorphous silicon-rich silicon carbide (a-Si_xC_{1-x}:H) because very large switching ratios can be obtained due to the large Schottky barrier heights in comparison to other silicon alloys. The large barrier heights enable a very low off-current to be obtained. A second feature of a-Si_xC_{1-x}:H is the ability to easily introduce and remove the defect states that are believed to initiate the switching process. In this paper, metal-semiconductor-metal (MSM) memory devices have been fabricated in hydrogenated amorphous silicon carbide. Instead of introducing defects by doping as has been done in previous experiments, ion bombardment has been used in this work to introduce defects into the a-Si_xC_{1-x}:H film. A switching ratio (range between the conducting (ON) and the non-conducting (OFF) states) of more than one order of magnitude higher than that for doped devices is reported. Also, the OFF state in previous reports does not necessarily mean the original unstressed conductance level of the device but in this work, the ability to switch the devices back to their original unstressed conductance levels is also reported. Implanted samples have exhibited digital switching unlike analog switching in doped devices. However, the mechanisms for this are yet to be fully investigated. Since ion implantation is an easy and convenient way of accurately controlling the densities and distribution of defects in semiconductors, it is expected that it should be a more viable tool for controlling the forming and switching voltages of these non-volatile memory devices.

K2.4
THERMAL CHEMICAL VAPOR DEPOSITION OF SILICON CARBIDE FILMS AS PROTECTIVE COATINGS FOR MICROFLUIDIC STRUCTURES. Ulrike Futschik, Spyros Gallis, James Castracane, Alain E. Kaloyeros, and Harry Efstathiadis, School of NanoSciences and NanoEngineering, The University at Albany-SUNY, Albany, NY; Leo Macdonald and Susan Hayes, Starfire Systems Inc, Watervliet, NY; Costas G. Fountzoulas, Army Research Laboratory, Weapons Material Directorate, Aberdeen Proving Ground, MD.

Amorphous silicon carbide (SiC) films were deposited on silicon and graphite substrates by thermal chemical vapor deposition technique (TCVD), at substrate temperatures ranging from 620 °C to 720 °C.

A novel single-source halide free precursor SP-4000, belonging to the family of polymethylsilanes (PMS), with the structure of $([\text{-SiH}_2\text{-CH}_2\text{-}]_n$, n = 2 - 8, was used as source. Argon was used, as both precursor carrier and dilution gas. Other reactants, such as hydrogen or hydrocarbons, were not used. The deposition yielded films with Si/C ratio of 1±0.05. The highest achieved growth rate was 86 nm/min. The modulus of elasticity and the nanohardness of the films were measured with the aid of a nanoindenter at various depths. To minimize the substrate effect, the average modulus of elasticity and nanohardness, were measured at a depth equal to 30% of the film thickness, were found to be 140 GPa±20 GPa and 7.0±1.0 Gpa, respectively. The results of the nanoindentation will be discussed in detail in conjunction with the microstructural analysis of the specimens. A 30% improvement in the film hardness was observed after post deposition annealing at 1200 °C in argon ambient. This was accompanied with a decrease of the hydrogen content of the films. Cross sectional TEM images showed a nanocrystalline phase of the annealed films consistent with the x-ray diffraction (XRD) data. In addition, the development of a viable TCVD SiC process presents significant opportunities in the nano/microsystems field. In particular, the ability to custom tailor the surfaces of microfluidic structures allows for the development of valves, pumps and channels for use in corrosive or high temperature environments. Initial results from the deposition of SiC films on prototype microfluidic components will be presented.

K2.5
WAFER BONDING TECHNQUE APPLIED TO SiC/SiC SYSTEM. G.N. Yushin, A.V. Kvit, and Z. Sitar, North Carolina State University, Department of Material Science and Engineering, Raleigh, NC.

SiC is a promising material for high power and high temperature electronics due to its high thermal conductivity and wide bandgap. There are more than 220 different polytypes of SiC, the band gap of which varies from 2.4 eV to 3.3 eV. Due to the difficulties in controlling the polytype change during the epitaxial growth, the formation of heterojunction devices using different SiC polytypes can be realized only by utilizing a wafer-bonding technique. In the present study we investigated the influence of temperature on the SiC/SiC bonding process. SiC wafers with RMS roughness of 1.5 nm were bonded in a dedicated ultrahigh vacuum bonding chamber. Successful fusion of wafers was observed at temperatures as low as 800°C under a uniaxial mechanical stress of 5 MPa. Cross-section transmission electron microscopy of the specimen bonded at 1100°C revealed parts of the interface where wafers were in intimate contact, while other parts contained an up to 2 nm thick amorphous carbon interlayer. The bonded SiC was found to retain its high crystalline quality; no extended defects emanating from the interface were observed within the sampling region. Detailed process parameters and results of the electrical measurements will be presented.

K2.6
STRUCTURAL AND PHOTOELECTRONIC PROPERTIES OF HYDROGENATED AMORPHOUS SILICON CARBIDE THIN FILMS PREPARED BY VHF-PECVD. Zhihua Hu, Xianbo Liao, Xiangbo Zeng, Yanyue Xu, Shibin Zhang, Hongwei Diao, Guangling Kong, Applied Physics Division, Institute of Semiconductors, Beijing, CHINA.

Two series of hydrogenated amorphous silicon carbidea-SiC:H films have been prepared by using very high frequency 60MHz plasma-enhanced chemical-vapor deposition VHF-PECVD with the gas mixture of methane and silane. The influence of the power density on the structural and photo-electronic properties of the films has been investigated with the methane gas ratio in the total gas flow rate ranging from 50 to 90%. The power density is an important parameter, which affects both the carbon content and the structures of the films. Under high power condition, the samples are Si-rich and the structure of them is described as a disordered amorphous silicon network in which hydrogen atoms are incorporated in the form of $SiCCH_2$ and $SiCCH_3$ entities and carbon atoms are in a sp^2 carbon-related configuration. The optical band gaps of these samples increase with the increase of the gas flow ratio. Under low power condition, the samples are carbon-rich and the structure of them is a mixed phase of amorphous Si and graphite-like C clusters. The optical band-gap of the samples decrease with the increase of the gas flow ratio.

K2.7
FIELD ENHANCEMENT MECHANISMS AND ELECTRON FIELD EMISSION PROPERTIES OF ION BEAM SYNTHESIZED AND MODIFIED SiC/Si HETEROSTRUCTURES. W.M. Tsang, S.P. Wong, Chinese Univ of Hong Kong, Dept of Electronic Engineering and Materials Science and Technology Research Centre, Hong Kong, CHINA; J.K.N. Lindner, Univ. of Augsburg, Institut für Physik, Augsburg, GERMANY.

The study of cold electron field emission (FE) properties of carbon containing materials has been a topic of intensive research efforts in the past few years. It was reported that good FE properties with a very low turn on field of about 1V/μm could be obtained from ion beam synthesized SiC/Si heterostructures and the good FE properties were attributed to field enhancement due to a surface morphology effect [1]. In this work, SiC/Si heterostructures were synthesized by high dose carbon implantation into silicon using a metal vapor vacuum arc ion source. Their electron field emission properties were studied and correlated with results from other characterization techniques including atomic force microscopy (AFM), conducting AFM, Fourier transform infrared absorption spectroscopy, x-ray diffraction, x-ray photoelectron spectroscopy, and transmission electron microscopy. It is clearly demonstrated that there are two types of field enhancement mechanisms responsible for the improvement of the electron field emission properties of these ion beam synthesized SiC/Si heterostructures, namely, the surface morphology effect and the local resistivity inhomogeneity effect. The dependence of the FE properties on the carbon implant dose and thermal annealing conditions could be understood in terms of these two field enhancement mechanisms. The FE properties from tungsten implanted SiC/Si heterostructures were also studied and discussed in conjunction with other microstructural characterization results. This work is supported in part by the Research Grants Council of Hong Kong SAR (Ref. CUHK4200/01E) and by the Germany-Hong Kong Joint Research Scheme of RGC, Hong Kong SAR and DAAD, Germany. [1] D. Chen et al, Appl. Phys. Lett. 72, 1926 (1998).

K2.8
TUNING THE SPECTRAL DISTRIBUTION OF p-i-n a-SiC:H DEVICES FOR COLOUR DETECTION. Paula Louro, Alessandro Fantoni, Miguel Fernandes, Reinhard Schwarz, Manuela Vieira, Electronics Telecommunications and Computer Dept, ISEL, Lisbon, PORTUGAL.

The aim of this work is to discuss the use of ZnO:Al/p(SiC:H)/i(Si:H)/n(SiC:H) structures as image and colour transducers. It concerns the structural, electrical and optical characterisation of the a-$Si_{1-x}C_x$:H films deposited by PECVD at low temperature. A systematic research on the optoelectronic properties of the layers under dark and different light illumination conditions was performed to understand its role on the output performance of the a-SiC:H based transducers. The efforts are focused mainly on doped n- and p-type layers at low doping levels with and without carbon. Carrier transport and collection efficiency are investigated from dark and illuminated current-voltage dependence and spectral response measurements under different optical and electrical bias conditions. Results show that the carrier collection depends on the optical bias and on the applied voltage. By changing the electrical bias around the open circuit voltage it is possible to filter the absorption at a given wavelength and so to tune the spectral sensitivity of the device. Experimental results were also compared with data obtained from a numerical simulation in order to understand the internal physical process related to the transport mechanism under light and dark conditions and to explain the bias control of the spectral response and the image and colour sensing properties of the devices.

K2.9
SPATIALLY RESOLVED PHOTO-AND THERMALLY STIMULATED LUMINESCENCE IN SEMI-INSULATING SiC WAFERS. Yu.M. Suleimanov, S. Lulu, I. Tarasov, S. Ostapenko, S.E. Saddow, University of South Florida, Tampa, FL; V.D. Heydemann, M.D. Roth, O. Kordina, M.F. MacMillan, Sterling Semiconductor, Tampa, FL.

We report on non-contact and non-destructive spatially resolved characterization of traps and luminescence centers in full-size 2 diameter 4H and 6H semi-insulating SiC wafers. Photoluminescence (PL) mapping and thermally stimulated luminescence (TSL) imaging was employed. The PL mapping was performed from room temperature down to 77K. Vanadium contaminated versus non-vanadium doped semi-insulating wafers were compared. PL and TSL intensities in V-wafers exhibit noticeable inhomogeneity across the wafer with axial symmetry. A luminescence pattern correlates with Hall activation energy, which shows a strong degradation at the wafers central area. In contrast, the PL and TSL in non-V wafers are quite homogeneous and reveal defects only at the periphery regions. PL and TSL spectroscopy were performed on the same wafers in the visible and infrared spectral regions. We have measured for the first time the infrared spectrum of V-related TSL, which replicates sharp lines of the V4+ inter-center transitions in SiC. TSL glow curves are measured by pumping a whole wafer with UV light followed by temperature increase from 80K to room at various thermal ramps. The glow curves show different TSL peaks in the visible and infrared luminescence bands. TSL spectral maximum at 2.2 eV corresponds to the trap with the ionization energy of about 100meV, which can be

attributed to a deep state of the nitrogen donors. The trap energy obtained from the TSL glow curve of V related band is 250meV. Low temperature PL spectrum of non-V wafers shows zero-phonon line at 1.346eV and local vibration mode accompanied with a broad phonon-assisted PL band at 1.18eV. TSL glow curves in these wafers show N-related peak at 107K and two additional high temperature maxima at 175K and 205K. TSL spectrum of the N-traps coincides with the 1.18eV PL band. The model of electron-hole transitions is discussed.

K2.10
EXISTENCE OF AN INTERFACE STATE AT THE STACKING FAULT IN 4H-SiC AND ITS IMPACT ON ELECTRONIC DEVICES.
M.S. Miao, Sukit Limpijumnong, and Walter R.L. Lambrecht, Department of Physics, Case Western Reserve University, Cleveland, OH.

The mechanism of the deterioration of SiC diodes by forward current was found to be correlated with an increasing number of stacking faults. Our first-principles calculations on a series of stacking fault models for 4H-SiC show the occurence of an interface band in the gap with maximum depth of 0.2 - 0.3 eV below the conduction band at the $\bar{M}$ point. This energy is much larger than the stacking fault formation energy which is found to be only a few meV/pair for 3C-, 4H- and 6H-SiC using the Anisotropic Next Nearest Neighbor Interaction (ANNNI) model. This indicates that the formation of the interface states and the trapping of electrons in these states can be a driving force promoting growth of the stacking fault area in an n-type sample. Radiationless recombination of electrons trapped at the stacking fault with holes is proposed to provide sufficient energy to overcome the partial dislocation motion barriers towards formation of additional stacking fault area in a device under forward bias.

K2.11
CHARACTERIZATION OF POROUS SiC SUBSTRATES AND THE EPILAYER STRUCTURES GROWN ON THEM. J. Bai, P. Gouma, M. Dudley, Department of Materials Science and Engineering, State University of New York, Stony Brook, NY; M. Mynbaeva, Ioffe Physical-Technical Institute, St. Petersburg, RUSSIA; and S. Saddow, Department of Electrical Engineering, University of South Florida, Tampa, FL.

SiC anodization is used to produce variable porous layers in single crystal substrates with the purpose of reducing undesirable growth artifacts, such as threading dislocations, on the thin films grown on top of these substrates. In order to evaluate the effectiveness of the porous "buffer" layers of SiC in reducing the defect density of the epilayers grown on them, systematic studies have been carried out using conventional and high resolution transmission electron microscopy and X-ray diffraction analysis techniques. These studies revealed the morphological features and defect densities of the as-received and of the anodized SiC. A comparison was made of the relative quality of the homo-epitaxial layers grown on the respective structures. This paper discusses the findings from these comparative studies and suggests ways for further improvement of then crystal quality.

K2.12
DEVELOPMENT OF ION ENERGY LOSS MEASUREMENTS IN $4H-$ AND $6H-SiC$ THANKS TO $SiCOI$ WAFERS OF PERFECT CRYSTAL QUALITY. Roberta Nipoti, Caterina Summonte, CNR-IMM Sezione di Bologna, Bologna, ITALY; Fabrice Letertre, SOITEC S.A., Parc Technologique des Fontaines, FRANCE.

The measurement of ion energy loss in crystalline semiconductor can be done by direct and indirect methods. The first consist in the measurement of the ion energy and charge state distributions of a monochromatic beam that has crossed a crystalline membrane. The latter consist in the ability to propose energy loss formulas that allow us to simulate the implanted species profiles in bulk crystal or to simulate the energy spectrum of monochromatic ions back-scattered from thin crystalline films on the top of a given substrate. This last indirect method is suitable in the case of MeV ions with atomic mass lighter than that of the species composing the semiconductor crystal and it was already successfully applied in the case of He^+ ions and Si-On-Insulator wafers. Here we propose to apply such a method also to the case of He^+ ions and the SiC-On-Insulator ($SiCOI$) wafers. This has been possible only thanks to the great progress made by the $SiCOI$ technology that gave us 50 mm diameter wafers of both the $4H-$ and $6H-SiC$ polytypes with thin homogenous thickness, flat and parallel surfaces, and perfect crystalline structure. UV-visible reflectivity spectra from different region of the same wafers were simulated to have the measure of the $4H-$ and $6H-SiC$ film thickness and the thickness homogeneity for each $SiCOI$ wafer. The Rutherford Back Scattering spectra of 0.8-2.3 MeV He^+ ions for random, < 0001 > axial, (10ø1Ø0) and (11ø2Ø0) planar channeling geometry were simulated to give the channeling and random energy losses of MeV He^+ ions both in the $4H-$ and $6H-SiC$ polytypes. The latter confirms curves already available in the literature, the former are original data.

K2.13
Abstract Withdrawn.

K2.14
SPECTROSCOPIC PROPERTIES OF CUBIC SiC ON Si.
Zhe Chuan Feng, Ian Ferguson, Georgia Institute of Technology, School of Electrical & Computer Engineering, Atlanta, GA.

In recent years, much progress has been made in the research and development (R&D) of hexagonal SiC based, in particular 6H and 4H, materials and devices because of the mature bulk crystal technologies. At the same time, great interests in cubic (3C) SiC grown on Si substrates are also kept because of advantages for this system. Efforts are continuing to improve the material quality because of large mismatches of 20% in lattice constants and 8% in thermal expansion coefficients between Si and 3C-SiC. Advanced materials characterization and analysis techniques are applying to promote the R&D in 3C-SiC/Si. For example, several years ago, it was reported that 3C-SiC/Si did not show room temperature (RT) photoluminescence (PL) emissions due to its indirect band gap nature. However, we report here the UV excitation RT PL-Raman spectrum on 3C-SiC/Si, showing the 2.3 eV luminescence due to the RT recombination over the 3C-SiC indirect band gap. A comprehensive investigation on a series of CVD 3C-SiC/Si has been performed via a combination of RT PL, Raman and infrared spectroscopy techniques. We performed extensive theoretical simulations on IR reflectance spectra of 3C-SiC/Si under various film conditions, including variable film thickness, damping level, doping carrier concentration, and surface roughness. Dozens of 3C-SiC films grown on Si by way of chemical vapor deposition (CVD) have been analysed by IR absorption and reflection technology as well as PL and Raman spectroscopy. Some unusual optical features were observed. A damping behaviour of the interference fringes away from the reststrahlen band is observed from some samples while the damping does not occur in high quality 3C-SiC/Si samples. Some samples showed dips at ~895 cm^{-1} at the top of the IR reflectance reststrahlen band. Different theoretical models were proposed and developed to investigate these features in comparison with experimental observations.

K2.15
EFFECT OF DOPING ON THE INDENTATION HARDNESS OF 4H-SiC. Ming Zhang, Case Western Reserve University, Department of Materials Science and Engineering, Cleveland, OH; H.M. Hobgood, Cree, Inc., Durham, NC; Khevna Shastri, P. Pirouz, Case Western Reserve University, Department of Materials Science and Engineering, Cleveland, OH.

The effect of doping on the Vickers indentation hardness, H_V, of silicon carbide has been investigated by indenting silicon- and carbon-terminated basal faces of 4H-SiC over the temperature range 20-1200°C. Over the whole range, the opposite faces of lightly doped 4H-SiC show a hardness anisotropy, with the Si-terminated face softer than the carbon-terminated face. In addition, over a certain temperature range, near-plateaus can be found in the hardness of the two faces. At lower temperatures, the heavily-doped 4H-SiC has a lower hardness than the lightly-doped crystals. The hardness anisotropy results are discussed in terms of the widely different mobilities of Si(g) and C(g) dislocations. In addition to the indentation tests, 2-beam bright-field and dark-field weak-beam TEM techniques were employed to investigate the configuration and dissociation of indentation-induced dislocations in 4H-SiC. The stacking fault energy of 4H-SiC (with a nitrogen concentration of $5\times 10^{16}cm^{-3}$) was estimated to be 13.5±3.5 mJ/m2; this is almost the same as the result previously obtained from dissociated dislocations introduced by compression tests.

K2.16
WHOLE-WAFER OPTICAL MAPPING OF DEFECTS IN INSULATING SILICON CARBIDE WAFERS .
M. Mier[a], J. Boeckl[a], D. Hill[b], S. Bertrand[c], E. Ramakrishnan[c], M. Roth[d], C. Balkas[e], and M. Nelson[a]; [a]Air Force Research Laboratory, Wright-Patterson AFB OH; [b]Wylie Laboratory, Dayton, OH; [c]OriginLab Inc., Northampton MA; [d]Sterling Semiconductor Inc., Sterling VA; [e]ChemIcon Inc., Pittsburgh, PA.

Plotting defect locations in insulating SiC presents a challenge because the total number of locations on a wafer is so large. We scan the wafer with visible light at an appropriate resolution and sort out transmissions appropriate for the defects we are looking for. Under these conditions, we find that voids and micropipes reduce the pixel transmission to 0.3 to 0.4. Sorting for this transmission reduces the number of pixels of interest to a manageable number, especially with recent progress in growing lower defect SiC. Now a commercial

plotting program can easily display defect locations within a circle representing the wafer boundary. We verify the defect locations by scanning electron microscope secondary electron images and scanning optical microscope visible-light images at several resolutions.

K2.17
Abstract Withdrawn.

K2.18
THERMAL STRESS AS THE MAJOR FACTOR IN SiC DEFECT GENERATION DURING PVT GROWTH. D.I. Cherednichenko, R.V. Drachev, I.I. Khlebnikov and T.S. Sudarshan, Univ. of South Carolina, Dept. of Electrical Engineering, Columbia, SC.

Micropipes and high dislocation density in SiC still represent the major obstacles for the commercial production and stable operation of high power SiC devices. In this work, generation of these defects during SiC PVT growth is explained as the thermal stress-induced phenomena. It has been demonstrated [1], that the dynamics of SiC PVT growth is completely determined by the self-congruent conditions at the surface of crystallization, which are defined by the vapor flux intensity and heat dissipation in the growing crystal. Moreover, the growth rate becomes limited only by the intensity of heat removal from the crystallization front when the crystal thickness exceeds 1.0 mm [1, 2]. Hence, the growth rate is positive and stable only if sufficient heat dissipation through the crystal is provided. In turn, this requires a correspondently increasing growth front-crystal backside temperature difference that can result in the associated enhancement of thermal stresses in the growing crystal. The analysis performed for various thermal conditions of 1×1SiC boule growth showed that the axial temperature distribution in the cylindrical crystal is almost linear that implies dT/dz=Const, while the radial temperature distribution at the growth front is significantly non-linear and, therefore, $(dT/dr)_{z=0}=f(r)$. Hence, $(dT/dr)_{z=0}$ represents the major factor in development of excessive thermal stresses in the growing crystal. In fact, the radial Von-Mises stress distribution at the growing surface of SiC is extremely non-uniform and exceeds the value of 1.0 MPa, i.e. the critically resolved shear stress at the growth temperatures. Thus the stress stimulated processes of defect generation and their rearrangement may take place in the growing crystal. In particular, possible mechanisms of micropipe formation due to dislocation coalescence [3] and processes of the material creepage [4] caused by the non-uniformity of thermal stress distribution under the high temperature conditions of SiC growth will be discussed. References: [1] D.I. Cherednichenko, Y.I. Khlebnikov, R.V. Drachev, I.I. Khlebnikov, T.S. Sudarshan, Mater. Sci. Forum 389-393 (2002) 95. [2] D. Hofmann, R. Eckstein, L. Kadinski, M. Kölbl, M. Müller, St. G. Müller, E. Schmitt, A. Weber, A. Winnacker, Mat. Res. Soc. Symp. Proc. 483 (1998) 301. [3] A.N. Stroh, Proceedings of Royal Society of London. Series A, Mathematical and Physical Sciences. 223 (1954) 404. [4] B.Y. Pines, Journal of Technical Physics (USSR), XXV(8) (1955) 1399.

K2.19
THERMAL PLASMA PHYSICAL VAPOR DEPOSITION OF NANOSTRUCTURED SiC COATINGS. Xinhua Wang, Keisuke Eguchi, Toyonobu Yoshida, Univ of Tokyo, Dept of Materials Engineering, Tokyo, JAPAN.

Silicon carbide coatings are of great scientific and technological interest, because silicon carbide combines unique physical properties, chemical stability and excellent mechanical properties. However, conventional chemical vapor deposition processes have the disadvantages of low deposition rates. In the present study, thermal plasma PVD with silicon carbide ultrafine powder as a starting material has successfully been applied to deposit SiC coatings. This study aims to try to correlate the microstructures, mechanical and thermoelectric properties with the processing parameters. Silicon carbide powder was fed into a hybrid plasma flame and completely evaporated. The generated high temperature vapor mixture was deposited on graphie, silicon and quartz substrates. Depending on the processing parameters, the films showed dense, columnar and dendritical morphology and nanocrystalline structures with the crystallite size in the range of 3-35 nm. The coatings were mainly consisted of β-SiC phase. The maximum deposition rate up to 400 nm/s was achieved. The hardness and elastic modulus evaluated at around 50 nm depth reached 37.1 GPa and 194.1 GPa, respectively. All the coatings were N-type semiconductors showing maximum Seebeck coefficient around -500 μVK^{-1} and the power factor around 10^{-4} $Wm^{-1}K^{-2}$ at 700°C, which were comparable with the results of specially doped SiC.

K2.20
STRANSKI-KRASTANOV GROWTH OF Ge QUANTUM DOTS ON SiC SUBSTRATES. C. Calmes, V. LeThanh, D. Bouchier, V. Yam, D. Débarre, R. Laval, Institut d'Electronique Fondamentale, Universite Paris-Sud, Orsay, FRANCE; S.E. Saddow, Center for Microelectronics Research, University of South Florida, Tampa, FL.

We report our first results using a UHV CVD system to form Ge quantum dots on off-axis SiC(0001) Si-face substrates. Pure silane and hydrogen-diluted germane (90:10) were used as precursors. The substrates were cleaned using the modified-Shiraki process. After introduction into the growth system, the native oxide layer was removed using silane with a flow rate of 5 sccm, a pressure of approximately 1.5E-4 Torr and a temperature between 1030 and 1080°C. The Ge quantum dots were then grown at a temperature of 750°C using 15 sccm of H2:GeH4 and at a pressure of approximately 4.5E-4 Torr. In-situ RHEED was used to monitor the surface morphology and transition to the Stranski-Krastanov regime. After silane cleaning the surface reconstruction was root 3 by root 3, as expected for SiC. After the introduction of germane the RHEED streaks became spotty indicating the formation of the Ge quantum dots. This transition occured very rapidly (in less than 30 seconds) due to the high lattice constant mismatch between Ge and SiC. Ex-situ scanning electron and atomic force microscopy were used to confirm the presence of the Ge dots. The dot diameter, height and density was in the range of 35-50 nm, 6-8 nm and 50-100 per square micrometer, respectively. The results of these experiments will be discussed in addition to on-going experiments to assess the degree of quantum confinement in these structures.

K2.21
FIRST-PRINCEPLES STUDY OF SiC/M (M=Ti AND Al) NANO-HETERO POLAR INTERFACES. Shingo Tanaka (Swing), Masanori Kohyama, National Institute of Advanced Industrial Science and Technology (AIST), Special Division of Green Life Tech., Osaka, JAPAN.

Metal-semiconductor nano-hetero interfaces are very important for development of high-performance electronic devices. Schottky barrier height (SBH) control and strong contact formation are essential issues. Recent SBH estimations for Si-terminated (Si-TERM) and C-terminated (C-TERM) 4H- 6H-SiC(0001)/M (M=Al, Ti, Ni, Pt) reveal that the SBHs depend on the interface structure. On the other hand, recent first-principles pseudopotential calculations of 3C-SiC/M (M=Ti and Al)[1-4] interfaces reveal that C-TERM (Si-TERM) interface has strong (weak) bonds, and the *p*-type SBH of C-TERM interface is smaller than that of Si-TERM one. The SBH relationship is the same tendency as recent experimental ones. In this paper, we discuss the interface structure effects (atom species dependence and orientation dependence) for 3C-SiC(111)/M and 3C-SiC(001)/M (M=Ti or Al) interfaces including up-to-date calculations of the 3C-SiC(111)/Al interfaces. Most stable atomic site of interfacial metal atoms is different from each interface. This feature can be explained by the interface morphology such as the number of back bonds, the neighboring atoms of interfacial atoms and the number and direction of surface dangling bonds. In both (111) and (001) interfaces, adhesive energy (*p*-type SBH) of C-TERM interface is larger (smaller) than that of Si-TERM one. SBH relationship is explained by following two factors: 1) the relative position of intrinsic band structures between two materials 2) the interface dipole derived from the charge transfer or the charge distribution itself at the interface. [1] S. Tanaka and M. Kohyama, Phys. Rev. B **64** 235308 (2001). [2] S. Tanaka (SWING) and M. Kohyama, Mat. Res. Soc. Symp. Proc. **640** H5.18.1 (2001). [3] M. Kohyama and J. Hoekstra, Phys. Rev. B **61** 2672 (2000). [4] J. Hoekstra and M. Kohyama, Phys. Rev. B **57** 2334 (1998).

K2.22
BAND GAP ENGINEERING OF SiCN FILM GROWN BY PULSED LASER DEPOSITION. Nae-Man Park, Sang Hyeob Kim, Gun Yong Sung, Electronics and Telecommunications Research Institute, Basic Research Lab, Daejeon, KOREA.

Silicon carbide (SiC), which is a wide band gap semiconductor, is mechanically strong and chemically inert, and of potential use in the fabrication of hard coating and electronic devices that have to operate at high temperature and in a harsh environment. It has been also studied for a blue light emitting diode (LED) and a power device because of the relatively easy formation of both n- and p-type materials. However, the tunability of band gap could widen its optoelectronic applications such as III-Nitrides. In this context, amorphous silicon carbon nitride (a-SiCN) alloys are very interesting materials ranging from the band gap of a-SiC (~2.5 eV) to insulating film of a-SiN (~5.0 eV). Most of the related works little show the continuous band gap tuning of a-SiCN in the wide range. In this work, the band gap tuning of a-SiCN was demonstrated in the range of 2.2 ~ 3.5 eV by pulsed laser deposition using mixed target. a-SiCN films were grown on silicon and quartz glass substrates at room temperature in the nitrogen atmosphere. Targets were fabricated by pressing the mixture of SiC, C, and SiN powders. The film stoichiometry could be varied by mixing ratio of target and the nitrogen gas pressure. Fourier transform-infrared (FI-IR), Auger electron (AES), and ultraviolet-visible (UV-VIS) spectroscopy showed

the bonding configurations and the band gap of the SiCN film. Structural properties of the films were also examined by scanning electron microscopy (SEM).

SESSION K3: CHARACTERIZATION/DEFECTS
Chairs: Adolf Schöner and Michael Dudley
Tuesday Morning, December 3, 2002
Room 206 (Hynes)

8:30 AM *K3.1
SOME CURRENT EFFORTS AT CHARACTERIZATION OF SILICON CARBIDE. W.J. Choyke, R.P. Devaty, University of Pittsburgh, Department of Physics and Astronomy, Pittsburgh, PA; and Collaborators.

In this talk we shall discuss a number of different experiments which attempt to enlarge our understanding of the structural, vibrational and electrical properties of polytypes of SiC. 1) Hot wall CVD is becoming a major means of producing thick and very clean epitaxial layers of 4H and 6H SiC. Films doped in the 10E13cm-3 range offer a particularly advantageous environment for the study of very thin local "foreign" polytype inclusions as well as midgap states. 2) The availability of relatively thick and pure 4H and 6H SiC crystals has renewed interest in getting more precise and detailed information on the bulk and vibrational properties of these polytypes. For this purpose new Brillouin scattering and neutron scattering experiments are in progress. In addition, a novel and relatively new technique, "X-ray Raman Scattering", has been used to obtain information on the lattice bands of relatively small single crystal samples of 3C SiC and 4H SiC. 3) Schottky barriers have been a puzzle for more than half a century. We shall report on a study of Schottky barriers in 4H and 6H SiC with (0001), (000-1), (1-100) and (1-210) faces. Contacts were made with W, Mo, Pt and Ti and C-V, I-V and internal photoemission measurements were made. 4) Finally, porous SiC is being revisited in both 4H and 6H SiC. Diagnostic techniques for the determination of pore formation and overall porosity and tailoring the porous SiC for special applications in CVD, MBE growth as well as for bone tissue engineering and medical applications will be discussed.

9:00 AM *K3.2
RECENT RESULTS ON DEFECT CENTERS IN SiC POLYTYPES. Gerhard Pensl, University of Erlangen-Nuernberg, Institute of Applied Physics, Erlangen, GERMANY.

The performance of electronic power devices based on silicon carbide (SiC) strongly depends on the quality of the semiconductor material employed. Extended crystal defects (e. g. dislocations and grain boundaries) and electrically active point defects, which may be introduced either during the crystal growth or subsequently by the processing (e. g. ion implantation and high temperature anneals), lead to a degradation of the device parameters. In order to optimize the material properties, intensive investigations are required to solve the many physical and technological problems. The understanding of diffusion, the solubility of dopants and the Hall scattering factor of free charge carriers is still fragmentary. The theoretical treatment of energetically deep defects is just starting and even more so, the physical interpretation of the nature of defects located in the middle of the band gap is difficult when applying the classical electrical analysis. In this contribution, we will report on recent experimental results of shallow or deep defect centers in bulk SiC as well as at the interface of MOS capacitors for different SiC polytypes.

9:30 AM K3.3
ION IMPLANTATION INDUCED DEEP DEFECTS IN N-TYPE 4H-SILICON CARBIDE. A.O. Evwaraye, University of Dayton, Physics Dept., Dayton, OH; S.R. Smith, University of Dayton Research Institute, Dayton, OH; M.A. Capano, Purdue University, Dept. of ECE, West Lafayette, IN.

Ion implantation has become the standard technique for selectively doping semiconductors. However, implantation causes lattice damage and local stoichiometric imbalance, which must be removed before a successful device can be fabricated. These conditions enhance the formation of intrinsic defects. The Z_1/Z_2 defects are examples of intrinsic defect centers (IRDC) formed by electron irradiation or by ion implantation. In order to repair the damage and activate the implanted species, the implanted materials are usually annealed at high temperature (1500 °C-1700 °C). Research results suggest that the annealing behavior of IRDC's depends on the mode of formation. In this work, n-type 4H-SiC epitaxial layers purchased from Cree Research, Inc. were implanted with either Ar or Al ions to a total fluence of 2×10^{16} cm^{-2} at 600 °C. The energy of the ions was 160 keV. The post implantation annealing was carried out in an Ar ambient at 1600 °C for various times. Schottky diodes were fabricated on the annealed specimens. Deep Level Transient Spectroscopy (DLTS), Thermal Admittance Spectroscopy, and Capacitance-Voltage measurements were used to study the ion implantation induced defects. The DLTS spectra of Ar-implanted 4H-SiC specimens revealed five defects at E_C-0.72 eV, E_C-0.41 eV, E_C-0.26 eV, E_C-0.12 eV, and E_C-0.11 eV, after the specimen had been annealed for 5 minutes at 1600 °C. The level at E_C-0.72 eV is most likely the Z_1 defect, though it's activation energy is close to that of the ET3 defect (0.66-0.74 eV), because ET3 is known to anneal out at 1400 °C. The DLTS spectra of Al-implanted 4H-SiC revealed only one complex defect level, at an energy of E_C-0.18 eV. The other defects that may have been formed by the Al implantation must have annealed out during the 15 minute anneal at 1600 °C. This defect, however, is stable after annealing at 1600 °C for 60 minutes. These results show that the defects formed in the two systems (SiC:Ar and SiC:Al) anneal differently. Details of these results will be discussed in this paper.

9:45 AM K3.4
EFFECTS OF STRUCTURAL DEFECTS ON DIODE PROPERTIES IN 4H-SiC. B.J. Skromme, K. Palle, Dept of Electrical Engineering and Center for Solid State Electronics Research, Arizona State University, Tempe, AZ; H. Meidia, S. Mahajan, Dept of Chemical and Materials Engineering and Center for Solid State Electronics Research, Arizona State University, Tempe, AZ ; W.M. Vetter, M. Dudley, Dept of Materials Science and Engineering, State Univ of New York at Stony Brook, Stony Brook, NY; K. Moore, S. Smith, T. Gehoski, Physical Sciences Research Lab., Motorola, Inc., Tempe, AZ.

The performance of rectifiers and other devices fabricated in 4H-SiC is often limited by the effects of structural defects in the epitaxial starting material. Here, we describe detailed investigations of the effects of several types of defects, including lamellar bands of 3C SiC incorporated into a 4H-SiC matrix during high temperature oxidation of layers on very heavily n-doped substrates, and the effects of isolated 1c screw dislocations. Schottky barriers were fabricated using Ti, Ni, or Pt metallization and characterized using current-voltage and capacitance voltage measurements and electron beam induced current (EBIC) imaging. Synchrotron white-beam X-ray topography (SWBXT) and cross-sectional transmission electron microscopy were used for structural characterization. Room and low-temperature photoluminescence were performed to detect lower band gap lamellae in the oxidized material on the heavily doped substrates. The Schottky barrier height of all three metallizations is uniformly reduced by 0.47 eV by the polytype conversion process during oxidation. High dislocations densities were found by SWBXT and the 3C layers were directly imaged by TEM. The 3C material is believed to be responsible for the lower barrier heights. The effects of screw dislocations were studied by correlating EBIC, SWBXT, and electrical measurements on individual diodes. While the number of dark spots observed in EBIC correlated directly with electrical ideality factors, the number of screw dislocations did not, suggesting that other defects are responsible for the electrical nonuniformities.

10:30 AM *K3.5
PROCESS INDUCED EXTENDED DEFECTS IN SILICON CARBIDE GRYSTALS GROWN VIA SUBLIMATION. Rositza Yakimova, Linkoeping University, Dept of Physics and Measurement Technology, Linkoeping, SWEDEN.

SiC crystals commonly contain defects that are related to the growth mode and the operation conditions, and remain to be eliminated. This paper will review grown-in extended defects in silicon carbide substrates and thick epitaxial layers, produced with sublimation growth technique. Epitaxial growth with high rate is used as a complementary tool for better understanding of defect formation at the early stage of growth. We will particularly focus on the growth conditions at which extended defects are likely to occur and on the identification of characteristic defects. We will also show an effect of defect reduction under certain process conditions, e.g. high lateral growth rate. Evidence will be presented for dislocation transformation from substrate to epilayer by glide and climb due to the higher surface energy at the intersection of the dislocation with growth steps. Evidences have been obtained that independently of the polytype and the surface polarity, there exists a transition layer between the substrate and the epilayer in which the crystal structure is highly disturbed either by formation of misfit dislocations, predominantly in growth on vicinal (off-axis) surfaces or by domain boundaries and polytype transformation during growth on atomically flat (on-axis) surfaces. The transition layer thickness may vary from 15 to 50 μm and it seems to depend on the growth rate if the initial surface treatment is identical. Furthermore, it will be shown that the surface morphology defects are particularly indicative for the presence of bulk defects and that their development during growth is accompanied with accumulation of large strain and lattice distortion in the material, this leading to multiplication of extended defects. Finally, the impact of the mass transfer mode (either diffusion limited or free molecular) during seeded sublimation growth on the uniformity of growth and the formation/termination of extended defects will be discussed.

11:00 AM K3.6
DEPENDENCE OF STACKING FAULT GROWTH DYNAMICS ON CURRENT THROUGH SiC PIN DIODES. R.E. Stahlbush, M.G. Ancona, Naval Research Laboratory, Washington, DC; J.B. Fedison, J.E. Tucker, S.D. Arthur, GE Global Research Center, Niskayuna, NY.

A major obstacle to bipolar SiC power-device development is the formation of stacking faults that are triggered by device operation. The stacking faults degrade the forward-biased conduction. The severity of the problem can be quite erratic. For example, the voltage increase at constant current can vary by more than an order of magnitude for diodes fabricated on the same wafer. Furthermore, the time scale for the appearance of the degradation can vary by more than an order of magnitude. While past work has shown that the electrical degradation is due to the growth of stacking faults, many details about the stacking fault growth and about how they degrade the electrical performance of devices are not well understood. In this presentation, the growth dynamics and the effects of the current density are examined by light emission imaging. PiN diodes in which the normally solid anode metal contact is replaced with a metal grid make it possible to directly observe the stacking faults. While typical operating current densities are ~100 A/cm^2, stacking faults will grow in sporadic spurts at currents < 0.1 A/cm^2. At 100 A/cm^2, many, but not all, of the stacking faults grow until they span the active region. At higher current density, many of the faults that stopped growing at 100 A/cm^2 start growing. New faults are nucleated and start growing as well. In all cases, once stacking faults have grown, their size never decreases. All stressing is done with sufficiently short current pulses and low enough duty cycles to keep the temperature in the diode's active region below 120 C. These behaviors suggest that the stacking fault growth is governed by locally varying stress. In regions with higher stress barriers, more excitation (provided by the electron-hole recombination) is needed for the stacking faults to start or continue growing.

11:15 AM K3.7
EXTENDED DEFECTS IN 4H SiC PiN DIODES. M.E. Twigg, R.E. Stahlbush, M. Fatermi, Naval Research Laboratory, Electronics Science and Technology Division, Washington, DC; S.B. Authur, J.B. Fedison, J.E. Tucker, General Electric, Niskayuna, NY; S. Wang, Sterling Semiconductor, Danbury, CT.

Light emission imaging (LEI) reveals the formation of extended defects in the 10 μm thick 4H SiC film in PiN diodes under forward voltage operation. In LEI images these extended defects appear principally as bright lines running parallel to the $2\bar{1}/bar10$ direction defined by the intersection of the vicinal (0001) plane with the device surface. Using site-specific plan-view transmission electron microscopy (TEM), we have found that the bright lines in LEI images occur where Shockley stacking faults intersect the active device region. TEM imaging also reveals the presence of 60 degree dislocations running parallel to the $2\bar{1}/bar10$ direction, though only in the top 1 μm of the 4H SiC film. It is likely that these dislocations have formed to relieve strains induced by doping effects. By comparing TEM images with dynamical image simulations, we have determined that the stacking faults also act to relieve compressive strain in the film.

11:30 AM K3.8
ACCURATE LATTICE CONSTANT AND MISMATCH MEASUREMENTS OF SiC HETEROSTRUCTURES USING HARMONIC X-RAY REFLECTIONS. Michael Dudley, XianRong Huang, SUNY at Stony Brook, Dept of Materials Science and Engineering, Stony Brook, NY; Philip G. Neudeck, J. Anthony Powell, NASA Glenn Research Center, Cleveland, OH.

The ability to reproducibly grow defect-free 3C SiC crystals could enable beneficial new SiC devices to be realized. However, the structural and electrical quality of the 3C polytype has previously been far inferior to commercial 4H and 6H SiC crystals. Recently, a "step-free surface heteroepitaxy" growth process has been developed that can achieve 3C SiC films completely free of double positioning boundaries and stacking faults on 4H and 6H SiC mesas [1]. Understanding the growth and defect formation mechanisms during 3C-SiC heteroepitaxial growth requires accurate characterisation of the films using high-resolution X-ray diffraction (HRXRD) and other techniques. Unlike conventional cubic semiconductor heterostructures, however, the epilayers and substrates of SiC (as well as III-nitride/sapphire) heterostructures may have different orientations, structures, or lattice symmetries. This usually makes the conventional HRXRD techniques unsuitable for lattice mismatch and strain relaxation measurements of heteroepitaxial films. In this presentation, we will demonstrate a harmonic-reflection based HRXRD method that can precisely determine the absolute lattice constants of SiC single crystals and films. Using this method, we have accurately measured the lattice constants of 4H and 6H SiC substrates and the 3C epilayers grown on them, and consequently their extremely small mismatch ($10^{-4} \sim 10^{-3}$). A series of important phenomena revealed by these measurements are mainly that: 1) no misorientation between the (0001) lattice planes across the 4H/3C or 6H/3C interface is detected within the instrumental resolution, confirming the 2D nucleation mechanism of the 3C epilayer from a flat coherent interface; 2) in-plane substrate-epilayer lattice mismatch always exists, but the unit cell of the 3C epilayer does not correspond to a completely relaxed cubic structure, indicating that the epilayer is partially strained with the film thickness up to 3 microns; 3) lattice mismatch varies for different regions, implying a complicated strain relaxation mechanism of 3C epilayers on various mesas.
[1] P.G. Neudeck et al., Materials Science Forum 389-393, 311 (2002).

11:45 AM K3.9
INFLUENCE OF ERBIUM DOPING ON THE FORMATION OF SILICON CARBIDE NANOCRYSTALS FOR OPTOELECTONIC APPLICATIONS. Spyros Gallis, Ulrike Futschik, Iftikhar Ul-Hasan, Mengbing Huang, Alain E. Kaloyeros, and Harry Efstathiadis, School of NanoSciences and NanoEngineering, University at Albany-SUNY, Albany, NY.

Rare earth doped materials are of great interest for a wide range of applications in optoelectronics. Erbium (Er) doped materials are of great interest, since trivalent bound Er shows an optical transition around 1.54 μm the standard wavelength in optical telecommunication systems. In the present work, we investigated the effects of Er incorporation on the growth of silicon carbide (SiC) nanoparticles, as well as the structural and optical properties of Er-doped nanocrystalline SiC thin films. Deposition of amorphous 500 nm to 1000 nm-thick SiC films on Si or graphite substrates was first achieved in a temperature range of 600 °C to 900 °C, by thermal chemical vapor deposition (TCVD), from a halogen-free precursor family of polysilyenemethylenes (PSMs) ([-SiH_2-CH_2-]$_n$, n = 2 - 8). The amorphous SiC films were implanted with Er ions to doses between 10^{13}-10^{15} cm^{-2} at room temperature. Post-implantation annealing at temperatures above 1000 °C was performed, leading to the formation of SiC nanocrystals with size of 10 to 100 nm. Characterization of the films was performed by x-ray photoelectron spectroscopy (XPS), x-ray diffraction (XRD), Rutherford backscattering spectrometry (RBS), Fourier transform infrared spectroscopy (FTIR), transmission electron microscopy (TEM), and four-point probe measurements. The film characteristics have been correlated with the optical properties of Er-doped SiC materials evaluated by optical absorption, spectroscopic ellipsometry, and photoluminescence measurements. Our work suggested that incorporating Er during the crystallization process could allow for better control over the size distribution of SiC nanoparticles. The influence of Er doping concentration on the optoelectronic properties of the materials was investigated.

SESSION K4: MOS TECHNOLOGY
Chairs: Marek Skowronski and Nelson S. Saks
Tuesday Afternoon, December 3, 2002
Room 206 (Hynes)

1:30 PM *K4.1
THE 4H-SiC/SiO_2 INTERFACE. J.K. McDonald[a,†], R.A. Weller[b,a] and L.C. Feldman[a]; [a]Dept. of Physics and Astronomy, [b]Dept. of Elec. Eng. & Comp. Sci., Vanderbilt Univ., Nashville, TN; G. Chung[‡], C.C. Tin and J.R. Williams, Physics Dept., Auburn Univ, Auburn, AL. Current address: [†]Sandia National Laboratories, Albuquerque, NM; [‡]Sterling Semiconductor Inc., Tampa, FL.

The interplay between interfacial chemistry and electronic defects is a classic semiconductor thin film problem, difficult to address experimentally because of the large differences in the sensitivity of electronic vs. physical interface probes. We have discovered a unique system, based in SiC, which clearly reveals this physical-electronic correlation. In particular, the relationship between nitrogen content and interface trap density (D_{it}) in SiO_2/4H-SiC has been quantitatively determined. Nitridation reduces D_{it} near the conduction band, changing the defect energy distribution within the gap. The results are consistent with a quantitative model in which these traps are cluster defects[1] with a near-continuum of energy levels. Nitrogen passivation of these traps proceeds by the dissolution of these clusters, atom by atom, as revealed through the kinetic analysis. This N passivated interface has established new values for low interface state density and high interface mobility in the 4HSiC-SiO_2 system.[2]
[1] R. Schorner, P. Friedrichs, D. Peters and D. Stephani, IEEE Elect. Dev. Lett. 20 241 (1999), V.V. Afanasev, M. Bassler, G. Pensl and M. Schulz, Phys. Stat. Sol. (A) 162 321 (1997).
[2] G.Y. Chung, et al. IEEE Elect. Dev. Lett. 22, 176 (2001).

2:00 PM *K4.2
NANOSCALE CHARACTERIZATION OF THE SILICON

DIOXIDE/SILICON CARBIDE INTERFACE AND THE EFFECT OF PROCESSING CONDITIONS. Kai-Chieh Chang, Carnegie Mellon University, Dept of Materials Science and Engineering, Pittsburgh, PA; Jim Bentley, Oak Ridge National Lab, Metals & Ceramics Div, Oak Ridge, TN; Lisa M. Porter, Carnegie Mellon University, Dept of Materials Science and Engineering, Pittsburgh, PA.

Silicon carbide is being intensively pursued around the world for high power and high temperature devices because of its wide band gap and other intrinsic properties such as its high bond strength, high electric field strength, and high saturation electron velocity. The fact that SiC forms an electrically insulating SiO2 layer on its surface by heating in an oxygen-containing atmosphere (analogous to Si) makes SiC a promising material for metal-oxide-semiconductor field effect transistors (MOSFETs). However, interface state densities at the SiO2/SiC interface remain approximately two orders of magnitude higher than those typically found at SiO2/Si interfaces, and carrier mobilities in the inversion channel of SiC-based MOSFETs are mysteriously low. Therefore, it is important to identify defects near the interface that may affect the electrical properties. Our studies using high resolution transmission electron microscopy (HRTEM) and electron energy loss spectroscopy (EELS) have shown that high C/Si ratios exist at distinct regions along SiO2/6H-SiC (0001) interfaces formed during wet oxidation at 1100 C. Prior to oxidation the substrates were cleaned using the complete RCA cleaning process. Following the cleaning process, the samples were immediately placed in a furnace maintained at 700 C with oxygen flowing to prevent graphitization of the SiC surface prior to increasing the temperature to that selected for oxidation. Oxidation at lower temperature (950 C) or a re-oxidation step at 950 C for 3 hrs following oxidation at 1100 C was found to reduce the interfacial C/Si ratio; however, each of these processes resulted in a slower decay of the C/Si ratio within the oxide layer adjacent to the interface. In this presentation we will show the C/Si ratio distribution across the SiO2/SiC interfaces as a function of processing conditions. We will also show correlations of these results with interface state density measurements and discuss the potential implications of these results on state-of-the-art SiC-based MOSFETs.

2:30 PM K4.3
ATOMIC SCALE OXIDATION OF SiC SURFACES. Fabrice Amy, Yves J. Chabal, Agere Systems, Murray Hill, NJ; Patrick Soukiassian, Commissariat l'Energie Atomique, DSM-DRECAM-SPCSI-SIMA, Saclay, FRANCE.

Semiconductor surface passivation is of central importance to micro- and opto-electronic device technologies, yet poorly understood at a fundamental level. For grow ultra thin oxides necessary for future devices, it is essential to understand the degree of homogeneity achievable and the nature of stress induced upon oxidation. Silicon carbide, featuring hexagonal (4H, 6H), cubic (3C) and rhomboedric phases, can be prepared with different surface composition, including carbon rich and silicon rich surfaces. SiC lattice spacing is 20% smaller than that of Si. Silicon rich phases such as the 3C-SiC(100)3x2 and 6H-SiC(0001)3x3 are therefore of special interest since they give the unique opportunity to investigate the role of surface morphology on oxygen incorporation into the surface. We have used infrared absorption spectroscopy, scanning tunneling microscopy, and core level synchrotron radiation-based photoemission spectroscopy to study oxygen interaction with the 6H-SiC(0001)3x3 surface and H_2O dissociation on the 3C-SiC(100)3x2. On the latter cubic surface, H_2O dissociation and subsequent thermally driven oxygen insertion is very similar to water oxidation of Si(100) surfaces. In contrast, O_2 reaction on the hexagonal surface is very different to what is observed on Si. Molecular oxygen dissociation occurs readily (< 1L), more than ten times faster than on silicon. Furthermore, oxygen is incorporated into the third silicon layer, far away from the dangling bonds only associated with the top adatom/trimer surface structures, in sharp contrast to silicon oxidation stabilized by the dangling bonds with subsequent insertion in the immediate backbonds. These results, based on the identification of the oxygen atom bonding sites, suggests that insertion into the third silicon layer is driven by the resulting relaxation of the highly strained 6H-SiC(0001)3x3 surface. [1] [1] F. Amy, H. Enriquez, P. Soukiassian, P.F. Storino, Y.J. Chabal, A.J. Mayne, G. Dujardin, Y.K. Hwu, C. Brylinski, Phys. Rev. Lett. 86, 4342 (2001).

2:45 PM K4.4
PHASE DIAGRAM FOR THE INTERACTION OF OXYGEN WITH SiC. Y. Song, Dept. of Physics, Vanderbilt U., Nashville, TN; and F.W. Smith, Dept. of Physics, City College of New York, NY.

We report on experimental studies of the interactions of oxygen with the Si- and C-terminated (0001) surfaces of 4H-and 6H-SiC at high temperatures T and low oxygen pressures. These interactions lead to the growth of SiO_2 at high O_2 pressures (passive oxidation), etching of the surface at lower pressures (active oxidation), and also to an enhancement of the surface segregation of carbon at still lower pressures. A unified $P(O_2)$-T phase diagram for the SiC + O_2 reaction is presented that helps to clarify the complicated behavior observed for this reaction and also provides an important link between surface studies of SiC at very low $P(O_2)$ and oxide growth studies at high $P(O_2)$. A thermodynamic model predicting these three distinct regions is outlined. The differences observed for the critical oxygen pressures and etching velocities for 4H- and 6H-SiC and for their Si- and C-terminated surfaces are discussed. Comparing these results for SiC with the active-to-passive transition previously observed for the Si + O_2 reaction, we note that an SiO_2 layer is stable on SiC at higher T and lower $P(O_2)$ than is the case on Si. Thus it is easier to grow an initial layer of SiO_2 on SiC than on Si under these conditions even though the growth of thick SiO_2 layers occurs more rapidly on Si at higher pressures. Finally, for both the 4H- and 6H-SiC polytypes of SiC it is observed that the C-terminated (0001) face not only oxidizes faster but also etches more rapidly in O_2 than the Si-terminated face.

3:30 PM *K4.5
SiO_2/SiC INTERFACE PROPERTIES ON VARIOUS SURFACE ORIENTATIONS. Hiroshi Yano, Tomoaki Hatayama, Yukiharu Uraoka, and Takashi Fuyuki, Nara Institute of Science and Technology, Graduate School of Materials Science, Nara, JAPAN; Tsunenobu Kimoto and Hiroyuki Matsunami, Kyoto University, Department of Electronic Science and Engineering, Kyoto, JAPAN.

SiC power MOSFETs have been expected in handling high power with low loss at high switching speed. However, they have a major obstacle of low channel mobility at the SiO_2/SiC interface, especially in 4H-SiC. Researches to elucidate the cause for the low channel mobility and its improvement have been carried out mainly on the (0001) face with an off-angle of several degrees toward [11$\bar{2}$0] direction. To overcome the situation of low channel mobility on (0001), we have successfully demonstrated that higher channel mobility can be obtained by using the (11$\bar{2}$0) face. The SiO_2/SiC interface properties may have correlation with bond configurations on different crystal orientations. In this talk, SiO_2/SiC interface properties on various crystal orientations, i.e. (0001), (11$\bar{2}$0), and (03$\bar{3}$8) faces, are given based on MOSFET and MOS capacitor characteristics measured at various temperatures. The (0001), (11$\bar{2}$0), and (03$\bar{3}$8) faces of 4H-SiC correspond to (111), (110), and (100) for the cubic structure, respectively. The (11$\bar{2}$0) face is perpendicular to the (0001) face, and the (03$\bar{3}$8) face is tilted by 54.7° toward [1$\bar{1}$00] from the (0001) face. Capacitance and conductance measurements of MOS capacitors at room and low temperatures revealed that the interface state density on (0001) drastically increases toward the conduction band edge, while those on (11$\bar{2}$0) and (03$\bar{3}$8) do not increase significantly. The smaller interface state density near the conduction band edge for (11$\bar{2}$0) and (03$\bar{3}$8) bring higher channel mobility and lower threshold voltage in MOSFETs compared to (0001). The temperature dependence of MOSFET performance was quite different among these faces. For example, a high channel mobility of 98cm^2/Vs on (11$\bar{2}$0) at 285K decreased to 35cm^2/Vs at 445K in proportion to $T^{-2.2}$. On the other hand, a low channel mobility of 5cm^2/Vs on (0001) increased to 19cm^2/Vs at 500K in proportion to $T^{2.6}$.

4:00 PM K4.6
OXIDATION KINETICS OF THE (11$\bar{2}$0) CRYSTAL FACE OF 4H-SiC. S. Dhar, Y.W. Song, A.B. Hmelo, L.C. Feldman, Vanderbilt Univ, Interdisciplinary Program in Materials Science, Dept. of Physics and Astronomy, Nashville, TN; R. Kalish, Technion, Physics Department and Solid State Institute, Haifa, ISRAEL.

The (11$\bar{2}$0) orientated surface or the a- face of 4H-SiC is technologically relevant as it promises improved performance for high power devices[1]. We report new studies of the controlled oxidation of a-cut SiC, an important process for fabrication of MOS devices. The growth kinetics of (11$\bar{2}$0) face (dry oxidation 950°C to 1150°C at atmospheric pressure) have been studied and compared to the more widely studied faces namely, the (0001) Si face and the (000$\bar{1}$) C face. Composition and thickness of the films have been measured by high-energy ion scattering combined with channeling and spectroscopic ellipsometry. Surface morphology has been evaluated using Atomic Force Microscopy. We have observed very large differences in the oxide kinetics among these crystal faces. The oxidation process has been modeled using a modified form of the well-known Deal-Grove model of Si oxidation[2]. Our results suggest that: 1) the solid state interfacial reactions depend on the surface stoichiometry of the crystal cut and 2) the diffusion controlled regime is governed by both in diffusion of oxidants and out diffusion of carbonaceous by-products. References: 1. Yano H., Hirao T., Kimoto T., Matsunami H., Asano K. and Sugawara Y., IEEE Electron Device Letters, 20, 611 (1999) 2. B.E Deal and A.S Grove, J. of Applied Physics, 36, 3770 (1965)

4:15 PM K4.7
AFTERGLOW THERMAL OXIDATION OF SILICON CARBIDE. Andrew M. Hoff, Arti Tibrewala, and Stephen E. Saddow, Department

of Electrical Engineering, University of South Florida, Tampa, FL.

We report, for the first time, the growth of thermal oxides on silicon carbide at temperatures below 900C using a novel afterglow thermal reactor. Flowing afterglows of microwave plasmas have been used for decades to study fundamental chemical reactions and in recent years they are employed as rich atomic oxygen sources for one of the principal techniques of polymeric photoresist removal in IC plants around the globe. The advantage of afterglow generation of a high flux reactive species is that microwave plasmas may be excited inside clean quartz tubing and further the plasma potential of such discharges is less than 10 electron volts, which is far below the sputtering threshold of most materials, lowering the chance of contamination. In our case, we have integrated an afterglow source with a vacuum furnace system. The substrates to be oxidized are placed in the hot zone of the furnace where they are exposed to the flowing afterglow at a pressure near 1 Torr. The afterglow chemistry generated from pure oxygen traveling through the source includes O2, atomic oxygen, and excited states of O2. All ions and electrons generated by the plasma source are confined to the microwave cavity limits and photons are excluded by trapping techniques. The wafers in the furnace are exposed to a rich chemistry of afterglow species that were generated by non-thermal means. The furnace temperature alone controls the chemical reaction between the afterglow species and the substrates.

We present the results of oxide growth on 4H and 6H silicon carbide substrates over a range of temperature. An example result is over 200 of film grown at 800C in 2 hours. Atmospheric processing in O2 at 1050C would require 14 hours to grow a similar thickness on SiC. Possible mechanisms and oxide properties will also be discussed.

4:30 PM K4.8
A SEMI-EMPIRICAL MODEL FOR ELECTRON MOBILITY AT THE SiC/SiO_2 INTERFACE. Nelson Saks, Naval Research Laboratory, Washington, DC.

Current state-of-the-art SiC power MOSFETs exhibit poor conductance due to high trap densities Dit at the SiC/SiO_2 interface. High electron trapping reduces the FET conductance by two (roughly equal) mechanisms: (1) Trapping reduces the density of free electrons available for conduction. (2) Scattering of inversion (free) electrons increases due to the higher density of trapped electrons, which reduces the mobility of the remaining inversion electrons. In this work, a rough semi-empirical model for scattering of inversion layer electrons at the SiC/SiO_2 interface is developed. The Hall electron mobility m_e and free electron density n_{inv} have been studied in multiple 4H- and 6H-SiC MOS devices and compared with the model developed here which is based on previous models of silicon MOS inversion layers. Hall effect data from silicon MOS devices with high Dit are also studied and reported for comparison. Only two electron scattering mechanisms are found to be important in SiC at 295K: (1) Above threshold, μ_e decreases slowly with increasing n_{inv} and effective surface field E_{eff}, consistent with well-known phonon-limited scattering. (2) At low values of n_{inv}, μ_e is found to *increase* with n_{inv}. This unexpected behavior is modeled as Coulomb scattering where the scattering increases with the number of trapped electrons but decreases with increasing n_{inv} due to increased charge screening. This scattering mechanism is more important in 4H compared to 6H-SiC because of higher electron trapping in 4H. (3) At very high values of n_{inv} and E_{eff}, it is expected that surface roughness scattering should begin to dominate because SiC surfaces are typically much rougher than silicon. However, we find no evidence for surface roughness scattering in any of the SiC devices measured, although it is readily apparent in the test high-Dit silicon device. Justification for this result and other details of the model and experimental data will be presented at the conference.

SESSION K5: POSTER SESSION
Chair: Stephen E. Saddow
Tuesday Evening, December 3, 2002
8:00 PM
Exhibition Hall D (Hynes)

K5.1
INFLUENCE OF CONDITIONS OF GROWTH ON STRUCTURAL AND ELECTRICAL PROPERTIES OF SEMICONDUCTOR SOLID SOLUTIONS $(SiC)_{1-x}(AlN)_x$ AT SUBLIMATIONS EPITAXY.
Gadgimet Safaraliev, Malik Kurbanov, Bilal Bilalov, Gulja Kardashova, Marat Gusejnov, Daghestan State University, Makhachkala, Daghestan, RUSSIA.

SiC and AlN form a uninterrupted series of solid solutions having width of the band gap from 3 up to 6eV, which have structure with direct gap at the certain structures. The solid solution $(SiC)_{1-x}(AlN)_x$ inherit unique mechanical, chemical and thermal silicon carbide properties. Besides the affinity of lattices parameters and thermal expansion coefficients of SiC and $(SiC)_{1-x}(AlN)_x$ allows to beget new heterojunctions on their basis with a low concentration at the heterointerface. The present work is devoted to study of growth processes of monocrystal epitaxial films of $(SiC)_{1-x}(AlN)_x$ from a gas phase by a sublimation method and to research of their structural, electrical properties depending on conditions of growth. The solid solutions $(SiC)_{1-x}(AlN)_x$ were raised on polytype 6- SiC substrates at temperatures 2300-2550 and pressure range from 2×10^4 to 8×10^4 Pa of nitrogen and argon gases mix in a growth zone from hot-pressed polycrystalline SiC-AlN tablets. The sublimation etching of substrate surface in superfluous Si-vapour and the subsequent growth epitaxial films $(SiC)_{1-x}(AlN)_x$ in continuous process has allowed to solve a problem of transitive layers unsoundness on a substratefilms border which arise as surface substrate carbon passivation during SiC dissociation. The growth velocity dependences and films structure on technological parameters were determined. It is determined that argon and nitrogen proportion and their partial pressure in growth zone have a significant influence on content of $(SiC)_{1-x}(AlN)_x$ solid solutions. The AlN concentration in $(SiC)_{1-x}(AlN)_x$ solid solution is increased till certain limits for given source in case of increase of nitrogen concentration in the growth zone. The growth velocity depends on nitrogen partial pressure too. The pressure increasing brings to growth velocity decreasing. Temperature increasing improves the structure layers perfection, however, degradation of the hetero-border as sequent of mutual diffusion is occurred. Nitrogen and argon partial pressure variation in the working chamber during growth procedure allows to control films electroconductivity types. The present work offers technology reception for making anisotropic heterostructure n-SiC/p-$(SiC)_{1-x}(AlN)_x$ during continuous mode of layers cultivation. The polytypic structure and film perfection depend on the AlN concentration. The layers with < 0.55 have homogeneous structure and 2 polytype. It is observed that $x \geq 0.65$ layers have block structure and strong structure heterogeneity on volume and on surface. In work results of researches of temperature dependence of specific electroconductivity $(SiC)_{1-x}(AlN)_x$ also are submitted. The influence of growth conditions on solid solutions electroconductivity is established.

K5.2
CONFINEMENT OF SCREW DISLOCATIONS TO PREDETERMINED LATERAL POSITIONS IN (0001) 4H-SiC EPILAYERS USING HOMOEPTIAXIAL WEB GROWTH.
Philip G. Neudeck, J. Anthony Powell. Glenn M. Beheim, and Emye L. Benevage, NASA Glenn Research Center, Cleveland, OH; Andrew J. Trunek and David J. Spry, OAI, Cleveland, OH.

Axial screw dislocations (including micropipes) are unpredictably distributed in high densities across all commercial 4H- and 6H-SiC wafers. While specialized individual device placement and patterning techniques have been employed to avoid some of these defects during device manufacture, these randomly located dislocations nevertheless still hinder the performance of 4H-SiC high power devices. If one could reproducibly confine these defects to the same positions on every SiC wafer, it might enable more capable and reproducible SiC devices. This paper reports initial demonstration of a growth process that confines screw dislocations to predetermined lateral positions in 4H-SiC epilayers. The process starts by dry reactive ion etching hollow enclosed-shape mesa patterns (such as a mesa laterally patterned to look like the letter O) into commercial on-axis (0001) SiC substrates. After the etch mask is stripped, homoepitaxial growth is carried out in pure stepflow conditions that enable thin cantilevers to grow laterally from the tops of mesas whose pre-growth top surfaces are not threaded by substrate screw dislocations [1]. When growth is continued, the cantilevers extending toward the interior of a hollow shape completely coalesce to form a diaphragm with a cavity beneath the coalesced webbed cantilevers. Each completely coalesced diaphragm surface studied by AFM exhibited either: 1) a screw dislocation growth spiral located exactly where final cantilever coalescence occurred, or 2) no growth spiral. The fact that growth spirals are not observed at any other position except the central coalescence point strongly indicates that substrate screw dislocations, initially surrounded by the hollow portion of the pre-growth mesa shape, are consolidated and relocated to the final coalescence point in the epilayer grown on top of the diaphragm. Factors for further process optimization will be discussed in the full paper. [1] P. G. Neudeck et al., Materials Science Forum Vols. 389-393, pp. 251-254 (2002).

K5.3
MODELING THE CRYSTAL GROWTH OF CUBIC SILICON CARBIDE BY MOLECULAR DYNAMICS SIMULATIONS.
Nicoletta Resta, Christopher Kohler, and Hans-Rainer Trebin, Institut für Theoretische und Angewandte Physik, Universität Stuttgart, GERMANY.

The crystal growth of a seed of cubic SiC in contact with the supercooled melt has been investigated by means of classical

molecular dynamics simulations. The crystallization process was studied with a set of supercells containing up to 2000 atoms, initially consisting in a 12 Å thick layer of crystalline SiC and a 18 Å thick layer of supercooled melt. The dynamic evolution of crystallization was then followed for several hundreds of nanoseconds with the simulated annealing technique performed at constant pressure and temperature. The atomic interactions were described by the Tersoff potential. We studied the dependency of the growth process on the crystallographic orientation of the crystalline/liquid interface by considering three different crystal planes, namely the {100}, {110}, and {111} planes. Within the pressure-temperature range considered in our simulations, we observed the crystal growth only for the {110} and the {111} orientations, but not for the {100} ones due to nonstoichiometric termination. The atomistic details of the crystal growth mechanism will be described and discussed.

K5.4
POLYTYPE TRANSFORMATION DURING SiC CRYSTAL GROWTH. S.I. Maximenko, I.I. Khlebnikov and T.S. Sudarshan, University of South Carolina, Columbia, SC.

Recent progress in the PVT growth of silicon carbide bulk crystals has resulted in single crystal wafers of the two most common polytypes, 4H and 6H. However, in spite of achievements in SiC bulk growth, the polytype inclusions along with micropipes and dislocations are the most common defects in SiC wafers. In 4H-SiC bulk crystals the most commonly observed polytype combination is 4H-15R-6H, and 6H-SiC boules contain mostly 15R polytype inclusions. In this report, the mechanism of possible polytype transformation and the influence of growth conditions on polytype transformation are discussed. The optical microscopy, high resolution elastic stress imaging technique, Raman spectroscopy, photoluminescence and chemical etching was used, for investigation of defect formation as a result of the polytype transformation in SiC bulk crystals.

K5.5
CHARACTERIZATION OF A CERAMIC-METAL-CERAMIC BOND: CHEMICAL VAPOR DEPOSITED (CVD) SILICON CARBIDE JOINED BY A SILVER-BASED ACTIVE BRAZING ALLOY (ABA). James V. Marzik, Morgan Advanced Ceramics, Inc, Hudson, NH; Toshi Oyama, Morgan Advanced Ceramics, Inc, Hayward, CA; Warren J. MoberlyChan, William J. Croft, Harvard University, Cambridge, MA.

Chemical vapor deposited (CVD) silicon carbide ceramic material was joined to itself via an air stable, silver-based active brazing alloy (ABA). Polycrystalline, theoretically dense silicon carbide (SiC) was deposited onto graphite substrates via the reductive pyrolysis of methyltrichlorosilane in a hot-walled chemical vapor deposition chamber. The resulting product can be considered a bulk material with deposit thicknesses in the range of 3 to 15 millimeters. An air stable joint between silicon carbide pieces was formed using a silver-based active brazing alloy. The area of the joint ranged from 1 to 10 square centimeters. The mechanical strength of the joint was measured as a function of surface finish of the ceramic. The microstructure and microchemistry of the interface was characterized using transmission electron microscopy (TEM), scanning electron microscopy (SEM), and electron probe microanalysis (EPMA). The effect of nitrogen doping on the microstructure of the interface was investigated.

K5.6
HOMOEPITAXIAL 4H-SiC FILMS GROWN BY MICROWAVE PLASMA CHEMICAL VAPOR DEPOSITION. Mitsuo Okamoto[a,b], Ryoji Kosugi[a,b], Shinichi Nakashima[a,b,c], Kenji Fukuda[a,b] and Kazuo Arai[a,b]; [a]National Institute of Advanced Industrial Science and Technology, Ibaraki, JAPAN; [b]Ultra-Low-Loss Power Device Technology Research Body, Ibaraki, JAPAN; [c]R&D Association for Future Electron Devices, Advanced Power Device laboratory, Tokyo, JAPAN.

Recent 4H-SiC homoepitaxial growth technique was progressed and high-quality 4H-SiC films were obtained by thermal chemical vapor deposition (thermal CVD) technique. However, so high growth temperature as 1600°C is required. Decrease of growth temperature will bring about more flexibility to 4H-SiC device process. Particularly, oxide, which is damaged over 1200°C, can be used during epitaxial growth. In this study, we attempted to grow SiC films below 1000°C, by microwave plasma CVD (PCVD). SiC films were grown on 8° off-axis toward [11-20] 4H-SiC substrates at 970°C. Qualities of grown films were significantly affected by the C/Si ratio. Relatively smooth SiC film was obtained at C/Si ratio of 175 which was much higher than that of conventional thermal CVD. The surface morphology of the SiC film showed oriented triangular shapes whose terraces inclined to [11-20] by 8°. The triangular shapes were supposed to be caused by macro step bunching. The confocal microprobe Raman scattering investigation was performed in order to confirm the poly-type of the grown film. It is known that the LO phonon-plasmon coupled (LOPC) peak becomes broader and shifts to higher frequency with increasing the free carrier density n [1]. In the spectrum for the grown film, a sharp line (964 cm^{-1}) corresponding to the LO mode of pure 4H-SiC was observed in addition to the broad LOPC peak line from the substrate. These results indicate that homoepitaxial growth of 4H-SiC has been attained below 1000°C. The electrical properties will be presented at the conference. This work was performed in collaboration with FED as a part of the METI project (R&D of Ultra-low-Loss Power Device Technologies) supported by NEDO. [1] S. Nakashima et al., Phys. Stat. Sol. (a) 162, 39 (1997)

K5.7
STEP-STEP INTERACTION ON VICINAL 4H AND 6H-SiC SURFACES. Hiroshi Nakagawa, Satoru Tanaka, and Ikuo Suemune, Research Institute for Electronic Science, Hokkaido Univ., Sapporo, JAPAN.

It is now well known that commercially available SiC surfaces reveal high density scratches and nanoscale roughness fluctuation and are smoothened by high temperature gas (H2, Ar, HCl) etching. The resulting surfaces after these treatments normally show regular step/terrace structures [1]. There are, however, very few reports concerning surface etching on vicinal SiC surfaces probably because of some difficulty in achieving step/terrace structures. In this presentation we will show clear step/terrace structures on both on-axis and vicinal SiC surfaces after high temperature (~1430°C) HCl/H2 gas etching. Surface physics such as step-step interaction and step bunching mechanisms are especially focused on. We found unique surface phenomenon on vicinal surfaces of polytype (4H and 6H) SiC, step bunching and step-step interaction. Stable steps with one-unit cell height appeared in most cases except for higher vicinal angle (3.5°) 6H-SiC surfaces, where steps with half-unit cell height were recognized. 4H-SiC always showed regularly spaced one-unit cell height steps regardless of high vicinal angles (~8°). Thus, step/terrace configurations are uniquely determined by its polytype and a vicinal angle. The surface free energy (SFE) of a vicinal surface, consisting of SFE of (0001) terrace sites, step free energy, and step-step interaction term, is considered to explicate the stability of step/terrace configurations. The last parameter, the step-step interaction, may effectively contribute to give rise to the half-unit cell stability on the vicinal 6H-SiC. Detailed structural characterizations by HRTEM, AFM, and STM as well as energetic calculations upon SFE will be presented. [1] S. Nakamura et al., Appl. Phys. Lett. 76, 3412(2000).

K5.8
NANOSCALE POLISHING OF SILICON CARBIDE AND SILICON WITH GAS-CLUSTER ION BEAMS. Vincent DiFilippo, Tufts Univ, Dept of Mechanical Engineering, Medford, MA; David Fenner, Epion Corp, Billerica, MA; Leonard Feldman, Vanderbilt Univ, Dept of Physics and Astronomy, Nashville, TN; James Hirvonen, Army Research Lab, Aberdeen Proving Ground, MD; Anil Saigal, Tufts Univ., Medford, MA.

Polishing SiC wafers is presently a challenging process and improved, vacuum-based methods are sought. Recently, the gas-cluster ion beam (GCIB) technique has been used to reduce the surface roughness of various semiconductor materials including Si and SiC to nearly theoretical limits and without apparent lattice damage. In GCIB, ionized clusters are accelerated towards a target substrate and their impacts produce a lateral sputtering effect which results in a net surface smoothing. A study was undertaken to explore various process conditions for GCIB smoothing of SiC wafers and to compare the surface science of the cluster-surface interaction for SiC with that for silicon. These semiconductor surfaces were exposed to a series of gas cluster ion treatments of varying ion fluence and acceleration, as well as source-gas choice including argon, oxygen, carbontetrafluoride and mixtures of these gases. The effect of beam incidence angle was investigated. After processing, atomic force microscope measurements (AFM) indicate a reduction of surface roughness and removal of pre-existing CMP polishing scratches from the SiC. Average roughness was reduced from about 10 angstroms to less than 4 angstroms after processing with oxygen clusters. Etch depths were measured by contact surface profilometer and found to be strongly dependent on cluster energy, species and incident angle. It was found that oxygen clusters produced a greater degree of smoothing while argon, carbontetrafluoride and mixtures of oxygen and carbontetrafluoride resulted in generally higher etch rates. RBS channeling measurements were also conducted, and showed that processing with a lower energy as the final exposure step of a series of doses minimized the amount of crystal lattice damage near the surface. Measured material sputtered from targets onto nearby surfaces determined the transfer of surface material and characterized the lateral sputtering. Comparisons of cluster processing of SiC with cluster processing of Si are provided here.

K5.9
STRUCTURAL AND ELECTRICAL PROPERTIES OF 200ns-PULSE EXCIMER LASER ANNEALED Al^+ ION IMPLANTED 4H-SiC. C. Dutto[a,b], E. Fogarassy[b], D. Mathiot[b], D. Muller[b], P. Kern[b], S. Joulie[c], J. Werckmann[c]; [a]STMicroelectronics, Tours, FRANCE; [b]Laboratoire PHASE-CNRS (UPR 292), Strasbourg, FRANCE; [c]Laboratoire IPCMS (GSI), CNRS, Strasbourg, FRANCE.

Silicon carbide (SiC) is a wide band gap semiconductor which presents unique material properties especially suitable for high temperature, high power and high frequency applications. However, SiC device fabrication has to face to various technological difficulties. Among them, one of the more crucial appears to be the doping step. The high melting point (T_M ~ 3100 K) and limited diffusion of impurities into SiC have greatly restricted the use of diffusion commonly employed in the silicon microelectronics industry to incorporate and activate the dopants. As an alternative to classical thermal heating, laser annealing (LA) was recently demonstrated to be suitable for the electrical activation of ion-implanted dopants in SiC. The use of high powerful pulsed excimer laser beams in the nanosecond duration regime allows to deposit a large amount of energy in very short time into the near-surface region, while maintaining the substrate essentially at room temperature. Under suitable conditions, the irradiation leads to the surface melting of SiC to a depth not exceeding a few hundred of nanometers, and its rapid solidification from the bulk. However, when working in the liquid phase, it appears very difficult to avoid surface degradation and change in the material stoechiometry.
In this work, we demonstrate the possibility to anneal the Al^+ ion-implantation induced damage into 4H-SiC by laser processing using a new XeCl excimer source of 200 ns pulse duration (~ ten times longer than the classical one). The laser irradiation conditions corresponding to solid phase annealing were estimated from thermal simulations and confirmed experimentally by SIMS measurements. The recovery quality of the lattice disorder as deduced from channeling RBS experiments, was investigated as a function of the number of the laser shots used (<100). XPS, AFM and TEM studies revealed that without additional SiC source material this ultra-fast thermal process allows to keep a surface stoechiometry ([Si]/[C]) near unity and prevents any strong surface degradation. Finally, the electrical activation of the laser annealed samples was studied by I-V and Hall effect measurements performed at various temperatures (300 - 900K) respectively on mesa pn junction diodes and classical Van Der Pauw structures.

K5.10
CRYSTALLINE EVALUATION BY ANNEALING TREATMENT OF 4H-SiC. Shin-ichiro Uekusa, Hiroshi Maruyama, Takayuki Goto, Department of Electrical and Electronic Engineering, Meiji University, Kanagawa, JAPAN.

Erbium (Er)-doped semiconductor is a potentially useful material for light-emitting devices in optical communication systems. since the intra-4f-shell transitions of Er ions cause sharp and temperature-stable luminescence in various host materials. 1.54μm, which corresponds to the minimum absorption of silica-based optical fibers. Photoluminescence (PL) from Er^{3+} in Er-doped narrow band gap semiconductors [e.g., silicon (Si)] has been reported, but the PL is weak and difficult to observe at room temperature (RT). In this work, Er ions were implanted into 4H-silicon carbide (SiC) material, which are useful host materials because they equip the wide band gap and improve the luminescence properties of Er^{3+} ions, and were characterized by PL measurements and Rutherford backscattering spectrometry channeling analysis. Er implantation energy was performed at 2MeV with a dose range of 1×10^{13} at RT. Following the ion implantation, these sample were annealed at ranging from 1400°C to 1700°C for 30 minutes using a rapid thermal annealing. Although the crystalline optimum annealing temperature investigated by Raman spectroscopy and electron spin resonance (ESR) was 1500°C for 30 minutes, the optimum annealing temperature for the intensity of PL were 1600°C for 30 minutes. Consequently, crystalline recovery does not necessarily lead to the influence of optimum luminescence intensity. Moreover, the dissociation of Si from the host material caused the decrease in the Raman intensity above 1600°C and then led to some damage in the host material. And, the crystalline recovery by annealing temperature also influenced the electrical property (I-V characteristics of Ni/4-H SiC). We report systematically the experimental results of PL, ESR, Raman, and I-V characteristics techniques.

K5.11
EPR STUDY OF THE CHANGES CAUSED BY HIGH TEMPERATURE ANNEALING OF 4H SiC. V.V. Konovalov, D. Alvarez, and M.E. Zvanut, University of Alabama at Birmingham, Dept of Physics, Birmingham, AL.

Application of SiC in electronic devices working at high temperatures requires detailed knowledge of its temperature behavior. This work investigates high purity as- grown 4H SiC after annealing in Ar or O_2 between 600 and 1700°C by using X-band (~9.5 GHz) electron paramagnetic resonance (EPR). EPR spectra were recorded at 4 K when excess shallow donors and acceptors are not ionized and paramagnetic. Unannealed samples did not show the presence of such typical impurities as B or N, but one broad spectral line associated with surface damage. After annealing at 1000°C the damage line was removed and three other centers were revealed. One was a carbon vacancy (V_C), another was a shallow B acceptor, and the third was not identified. After the surface damage signal was removed, the concentration of the remaining paramagnetic centers was less than 10^{15} cm^{-3}. Unlike the radiation-induced carbon vacancy reported by others, V_C in our sample remained stable between 1000 and 1400°C. However, annealing between 1500 and 1700°C decreased V_C and increased B, both by an order of magnitude. After illumination of the 1700°C annealed sample with 578 nm light, the EPR signal of V_C reappeared with approximately the same intensity as the 1000°C annealed sample. This indicates that annealing changed the charge state of the carbon vacancy but did not remove it from the substrate. Data from our previous photo-EPR study of unannealed SiC suggests that the energy level of V_C is 0.9 eV above the valence band edge. Thus, the disappearance of V_C and increase of B imply that the Fermi level position changes during annealing. This work is supported by the Office of Naval Research.

K5.12
TRANSPORT MECHANISMS IN FOCUSED ION BEAM ASSISTED OHMIC CONTACTS TO P-TYPE 6H-SiC. Agis A. Iliadis, Luohong Liu, Univ of Maryland, Dept of Electrical and Computer Eng, College Park, MD; K.A. Jones, Army Research Lab, Adelphi, MD.

The current transport mechanism in non-annealed Ohmic contact metallizations on p-type 6H-SiC made by using focused ion beam (FIB) surface-modification and direct-write metal deposition will be reported, and the properties of such focused ion beam assisted contacts, will be discussed. The process of focused ion beam assisted metallizations uses a Ga focused ion beam to modify the surface of the semiconductor with different doses, and then introduces an organometallic compound in the Ga ion beam, to effect the direct-write deposition of a metal on the modified surface. Contact resistance measurements by the transmission line method, produced values in the low 10-4 Ohm cm2 range for surface-modified and direct-write Pt and W non-annealed contacts. An optimum Ga surface-modification dosage window is determined, within which the current transport mechanism of these contacts was found to proceed mainly by tunneling through the metal-modified-semiconductor interface layer.

K5.13
STABLE OHMIC CONTACT FOR P-TYPE 6H-SiC USING Ti/Al AND TiN/Al THIN FILMS. Byung-Teak Lee, Jong-Yoon Shin, Chonnam Natl Univ, Dept of Materials Science and Engineering, Gwangju, KOREA; Sang-Yoon Han, Jong-Lam Lee, Pohang Univ of Science of Technology (POSTECH), Dept of Materials Science and Engineering, Pohang, KOREA.

Interfacial reactions, surface morphology, and I-V characteristics of Ti/Al/6H-SiC and TiN/Al/6H-SiC were studied, before and after high temperature annealing. The surface smoothness of annealed Ti/Al/SiC and TiN/Al/SiC samples were not significantly affected by the heat treatment up to 900°C, whereas that of the Al/SiC samples seriously deteriorated after the annealing. The I-V measurement indicated improved contact resistance in the case of Ti/Al/SiC contact, when compared with the Al/SiC contact. The transmission electron microscopy observation showed little micro-structural change in the 500°C samples. The Al layer reacted with the SiC substrate at 900°C and formed an Al-Si-C ternary compound at the metal/SiC interface, which is very similar to the case of Al/SiC interface. These results indicate that the Ti and TiN films can be utilized to stabilize the Al/SiC contact by protecting the Al layer from the potential oxidation and evaporation problem, while maintaining proper ohmic properties. Key words : ohmic contact, p-SiC, Ti/Al, TiN/Al

K5.14
LOW TEMPERATURE FORMATION OF Ni SILICIDE CONTACTS TO SiC. Chris Deeb and Arthur H. Heuer, Case Western Reserve University, Cleveland, OH.

Thermodynamically stable Ni silicide electrical contacts can be formed on n-type 6H-SiC by reacting a sacrificial LPCVD silicon layer with sputtered Ni at 300° C for 12 hours; nickel is used as an etch mask for the sacrificial silicon layer. The resulting Ni silicide film has been characterized by grazing incidence x-ray diffraction (XRD) and transmission electron microscopy (TEM). Room temperature contact resistivities were ohmic, 9.6×10^{-5} to 8.5×10^{-4} Ωcm^2. Contacts aged at 600° C for up to 300 hours in air remained ohmic and showed

much reduced room temperature contact resistivities, 7.6×10^{-5} to 2.7×10^{-6} Ωcm^2.

K5.15
PHOTOCHEMICAL PATTERN ETCHING OF SILICON-CARBIDE BY USING EXCIMER LASER AND HYDROGEN PEROXIDE SOLUTION. Dai Sasaki, Masataka Murahara, Tokai Univ, Department of Electrical Engineering, Hiratsuka, Kanagawa, JAPAN.

A circuit pattern etching of a Silicon-carbide(SiC) surface was conducted with KrF excimer laser irradiation in the presence of the HF and H_2O_2 mixed solutions. SiC has excellent properties of a high hardness, high melting point, wide band gap, high resistance to radiation and chemical stability. Therefore, this material has come to attract attention as an integrated circuit material for high resistance to environment. But a micro-machining of the material is very difficult by the photo-lithography because of the chemical stability. Then, we developed the new etching method that SiC surface was photo oxidized with H_2O or H_2O_2 by using excimer laser irradiation, and it was etched by HF water solution. In this experiment, these mixed solutions are poured into the thin gaps with capillary phenomenon between the Al_2O_3 glass and the SiC surface. Then, patterned excimer laser light is irradiated on the SiC surface, and H_2O or H_2O_2 in the reaction solution is photodissociated, and active oxygen is reacted with SiC. And CO_2 and SiO_2 are formed only a patterned exposure part forcibly, and oxidized layer is formed. In this chemical reaction, the CO_2 is evaporated and the SiO_2 is remained on the sample surface. And then SiO_2 layer is dissolved by HF water solution. Thus, etching is conducted by the repetition of the forced oxidization of SiC and the dissolving of the oxidized layer. In this experiment, the most effective conditions are 20% of H_2O_2 water solution, 15% HF water solution and 256mJ/cm^2 of KrF excimer laser. The etching depth is 80Å at a laser shot number of 10000. This etching depth was effective than an ArF excimer laser (256mJ/cm^2, 193nm) irradiation of 50Å. In these results, SiC circuit pattern etching became possible as in Si lithography.

K5.16
THE EFFECT OF ANNEALING ON HIGH-RESISTIVITY AND SEMI-INSULATING 4H-SiC. S.R. Smith, University of Dayton Research Institute, A.O. Evwaraye, University of Dayton Physics Department; W.C. Mitchel, Air Force Research Laboratory, Manufacturing and Materials Directorate.

We have examined specimens of high-resistivity, and semi-insulating, 4H-SiC before and after annealing at 1600 celsius, using Optical Admittance Spectroscopy. We have found enhanced ultraviolet response in most specimens, and enhanced activation of previously undetected V impurities. Peaks believed to be attributable to complex V-related defects were greatly reduced by annealing. The annealing was in addition to a thermal oxidation at 1150 celsius for 4 hours. The purpose of the oxidation was to remove deep levels known to be present in polished SiC. Transition metal impurities in these bulk specimens were detected by SIMS. In specimens where Ti was not detected by SIMS, no further activation of Ti centers was detected by Optical Admittance Spectroscopy.

K5.17
DEFECT ACCUMULATION AND RECOVERY IN ALUMINUM IMPLANTED 4H- AND 6H-SiC. W. Jiang, W.J. Weber, Pacific Northwest National Laboratory, Richland, WA; Y. Zhang, Ångström Laboratory, Uppsala University, Uppsala, SWEDEN.

Polytypes of silicon carbide (SiC) represent a series of wide-bandgap semiconductor materials that have attracted extensive investigations because of their great potential for a wide range of electronic applications. Aluminum implants provide an outstanding p-type dopant in SiC due to low activation energy; thus, it is important to understand implantation-induced damage and its recovery in SiC for developing high-quality electronic devices. Damage accumulation has been studied in single crystals of 4H- and 6H-SiC implanted with 1.1 MeV Al_2^{2+} ions at temperatures from 150 to 820 K over a range of fluences. The disorder on both the Si and C sublattices has been simultaneously studied in situ using a combination of 0.94 MeV D^+ Rutherford backscattering spectrometry and nuclear reaction analysis in channeling geometry. Multiple crystallographic axes have been used to determine the disordering behavior along different orientations. The relative disorder on both sublattices follows a nonlinear dependence on ion fluence. Considerable dynamic recovery of the Si and C defects is observed during ion implantation at room temperature and higher. There is a significant dose-rate effect on the disordering rate at implantation temperatures near 500 K. In addition, in-situ isochronal annealing (20 min) has been performed over temperatures from 170 to 870 K. After each annealing step, the residual disorder is determined by the same ion-beam methods. Some damage recovery is observed at room temperature on both the Si and C sublattices in the specimens implanted at low temperatures. Damage recovery at higher temperatures occurs in several stages. The dependence of dynamic/thermal recovery on implantation/annealing temperature over a full range of damage levels in 4H- and 6H-SiC will be presented and discussed.

K5.18
DAMAGE RECOVERY OF Al IMPLANTED 6H-SiC BY NOVEL "CAP AND ANNEAL" PROCESS. V.N. Kulkarni, S.S. Hullavarad, R.D. Vispute, J.A. McGee, S.R. Harmon, D.J. Wagstaffe, and T. Venkatesan, CSR, Department of Physics, University of Maryland, College Park, MD; K.A. Jones and M.H. Ervin, Army Research Laboratory, Adelphi, MD.

High performance power devices need good quality p-type SiC with low defect densities and smooth surface morphology. Since most dopants have very small diffusion coefficient in SiC, ion implantation and subsequent high temperature annealing (1400-1800°C) to remove the ion induced damage remains the only choice for doping. However the high temperature annealing process results in increased surface roughness and change in surface composition of SiC due to preferential evaporation of silicon from its surface. In order to circumvent this problem of surface degradation we have followed a novel "Cap and Anneal" process to remove the ion implantation damage in SiC without causing alterations in surface morphology and composition due to high temperature annealing. 6H-SiC crystals were implanted with Al at various energies to achieve uniform concentration of $1x10^{19}$ atoms cm^{-3} up to a depth of 3500Å. The surface of implanted samples was encapsulated first with 2000Å of AlN and subsequently with 2000Å of BN films using pulsed laser deposition technique. Samples were annealed at various temperatures in the range of 1400-1700°C after which the caps were removed. The initial damage induced by Al implantation and its recovery as a function of annealing temperature was studied by ion channeling technique. The channeling studies revealed a good recovery of SiC crystal without causing degradation in surface composition and morphology. These results will be presented and discussed in the context of future development of high-temperature and high-power SiC-based device technologies.

K5.19
THE EFFECT OF CHANNEL RECESS AND PASSIVATION ON 4H-SiC MESFETS. Ho-Young Cha, Christopher I. Thomas, Goutam Koley, Lester F. Eastman, Michael G. Spencer, Cornell University, Dept of Electrical and Computer Engineering, Ithaca, NY.

SiC MESFETs have emerged as promising high power microwave devices due to unique material properties such as high saturated electron velocity, high breakdown field, and high thermal conductivity. Channel recessed 4H-SiC MESFETs have demonstrated excellent small signal characteristics and the effect of Si_3N_4 passivation on these devices has been studied in this work. The layer structure for the devices consisted of a semi-insulating 4H-SiC substrate, a 0.25μm p-type buffer layer doped $< 5\times10^{15}$cm^{-3}, and a 0.26μm n-type channel layer doped $N_d = 2\times10^{17}$cm^{-3}. The source and drain regions were implanted with phosphorous and the channel region between source and drain was etched by 0.06μm to improve small signal characteristics. Channel recess resulted in lower saturation current but higher breakdown voltage, which would maintain similar output power level. The saturated current of 250~270mA/mm and a maximum transconductance of 40~45mS/mm was measured for channel recessed devices with a gate length of 0.45μm. The 3-terminal breakdown voltages V_{ds} range from 120V to more than 150V, depending on gate-drain spacing. These devices have demonstrated excellent F_t and F_{max} of 14.5GHz and 40GHz, respectively. Especially, F_{max} was significantly improved compared to the devices without channel recess (with F_{max} of 28GHz). These devices were passivated with PECVD Si_3N_4 film. Although the saturated current became lower after passivation, the output power and PAE were increased by 40% and 16%, respectively, in CW power measurement. It can be explained by less current dispersion examined after passivation. It is clear that the passivation reduces the surface effects and enhances the RF power performance by suppressing the instability in DC characteristics. We performed measurements on stressed devices using surface probing techniques, which also support the improvement after passivation. Devices with a short gate length will be studied on a thin channel layer with higher doping concentration and the results are expected by the time of this conference.

K5.20
HAZARDOUS GAS DETECTION USING SILICON CARBIDE SENSORS. C.I. Muntele, D. Ila, I.C. Muntele, R.L. Zimmerman, Alabama A&M University, Center for Irradiation of Materials, Normal, AL.

Real-time detection of hazardous gas leaks is important for personnel safety, but also for economic reasons such as process monitoring, reliability, and control. The automobile industry is perhaps the largest user of gas sensors, where oxygen sensors based on conductivity

changes in zirconium and titanium oxides are used for monitoring the air-to-fuel ratio of engines exhaust. For cases where hydrogen- or hydrocarbon-based gaseous species are involved, a relatively successful formula has been developed in the past few years for a sensor based on silicon carbide either coated or implanted with palladium. The palladium is known for its ability of taking hydrogen from its gaseous compounds, and then releasing it in the substrate material, modifying the electrical conductivity of the later by a measurable amount. Silicon carbide was proven a good replacement for silicon, because of its excellent stability at temperatures as high as 800°C. Stable configurations of Schottky diodes and MOS structures have been demonstrated to detect hydrogen. We demonstrate here an n-p-n structure obtained by introducing palladium into the silicon carbide substrate using an elevated temperature ion implantation process that reduces the damage level incurred to the crystalline lattice. Our devices have shown sensitivity to small fractions of hydrogen, methane, propane and acetone in argon and nitrogen environments even at room temperature, although the sensitivity increases with the elevation of the temperature at which the sensor works. Among the qualities of our devices are their compact size (millimeters), extremely low power requirements, and stability with time.

K5.21
FABRICATION OF NOVEL OPTICAL HIGH-TEMPERATURE SENSOR USING SiC THIN FILM GROWN ON SAPPHIRE SUBSTRATE. Lin Cheng, Andrew J. Steckl, Nanoelectronics Laboratory, University of Cincinnati, Cincinnati, OH; James D. Scofield, Air Force Research Laboratory, Wright-Patterson Air Force Base, OH.

An optical high temperature sensor, which is rugged, compact, stable, and can be easily fabricated, is developed by using 3C-SiC thin film grown on sapphire substrate at relatively low temperature (<1200°C) by low pressure chemical vapor deposition. The growth of a highly uniform 3C-SiC with a highly stable and impermeable thin film structure as well as a smooth SiC/sapphire interface is the essential step in producing a sensor with the required long-term stability. The thickness of 3C-SiC film was in the range from 0.5 μm to 3 μm. Crystallinity, surface morphology and roughness of 3C-SiC films were examined by x-ray diffraction (XRD), scanning electronic microscopy (SEM) and atomic force microscopy (AFM) respectively. A fiber spectrometer was used with a broadband white light source for reflection measurements on 3C-SiC-based temperature sensor. The sensor was operated in the range from 23°C to 500°C. The initial results show that the measured shift in resonance minima, λ_m, versus temperature fits a linear function. For the sensor with 1.5 μm thick SiC thin film, shifts of 11.24 nm, 12.83 nm and 14.91 nm in resonance minima have been observed at minimal resonance wavelength near 550 nm, 601 nm and 662 nm, respectively. A linear fit to λ_m near 601 nm versus temperature provides a thermal expansion coefficient, κ_Φ, of $(4.9\pm0.15) \times 10^{-5}/°C$. A larger shift in resonance minima at longer wavelength indicates a higher temperature resolution of the sensor. A capability of providing a ±5°C accuracy is obtained at 500°C. The effect of 3C-SiC film thickness variation on the performance of temperature sensors will be discussed.

K5.22
Abstract Withdrawn.

K5.23
DUAL-METAL-PLANAR RECTIFIERS ON SILICON CARBIDE USING Ti AND Ni_2Si AS SCHOTTKY BARRIER METALS. Fabrizio Roccaforte, Francesco La Via, Salvatore Di Franco, Vito Raineri, CNR-IMM, sezione di Catania, Catania, ITALY.

Among power devices in SiC, Schottky rectifiers are those better approaching the trade-off curve on-resistance versus breakdown voltage. In order to minimize the power dissipation of a Schottky diode, both low forward voltage drop and low leakage current are required. Since these conditions cannot be achieved by using a single Schottky barrier, new design concepts are needed to improve the device performances. In this work, dual-metal-planar (DMP) Schottky diodes, using titanium (Ti) and nickel silicide (Ni_2Si) as Schottky metals, are presented. The DMP diodes were fabricated on both 6H- and 4H-SiC wafers, purchased by CREE, with a n-type epilayer doping concentration in the range $0.3\text{-}1\times10^{16}$ cm^{-3}. The dual-metal contact was formed by standard photolitographic processes and selective metal etches, in order to obtain micrometric Ti stripes surrounded by a Ni_2Si contact. Under forward bias, the I-V characteristics of the rectifiers were very close to those of the Ti diodes, i.e. the ones with the lowest barrier height. On the other hand, their reverse leakage current was comparable to that of the Ni_2Si diode, i.e. the one with the lowest reverse leakage current. The current transport can be explained as follows. In forward bias, the system essentially works as parallel diodes with different barrier heights, thus meaning that only the low Ti Schottky barrier is working. Under reverse bias, instead, the pinch-off of the low barrier region by the high barrier regions occurs. The depletion layer at the Ni_2Si/SiC junction spreads into the region underlying the Ti stripes. Hence the conduction channels under the Ti are pinched-off and the carrier transport is ruled by the high barrier metal (Ni_2Si). The on/off ratio of the DMP diodes (calculated at 1 V and -100 V) improved with respect to the single metal diodes and was 2.3×10^4 in 6H-SiC and 1.4×10^2 in 4H-SiC. This difference may be attributed to the difference in the barrier height of Ti and Ni_2Si in these SiC polytypes.

K5.24
3C-SiC/6H-SiC HETEROJUNCTION DIODES. A.A. Lebedev, A.M. Strel'chuk, N.S. Savkina, E.V. Bogdanova, A.S. Tregubova, A.N. Kuznetsov, A.F. Ioffe Physiko-Tekhnical Institute, Laboratory Physics of Semiconductor Devices, St. Petersburg, RUSSIA.

In the present paper investigation of electrical characteristics of p– - 3C-SiC /n+ - 6H-SiC heterojunction grown by sublimation in vacuum was done. Low doped (Na-Nd= 3-4x 1016 cm-3) layers of p-3C-SiC was grown by SEV directly on (0001)Si plane of 6H-SiC Lely substrate (Nd-Na ~3 x 1018 cm-3). On the top of this layer was grown by SEV strongly doped p-3C-SiC layer for ohmic contact formation. Diode mesa structures with diameter 500 μm were produced by plasmo-ion etching in SF6. I-V characteristics of the investigated diodes has exponential forms. Typical capacitance – voltage (C-V) characteristics of diodes were linear in coordinates 1/C2 – V. This mean that obtained pn junction was abrupt. In spectrum of electroluminescence (EL) of this diodes presents green band close in spectrum position to band of free-exiton annihilation in 3C-SiC. But maximum position of this line was shifted to short- wave region of the spectrum on about 0,05-0,07 eV in contrast with typical position of exiton band in 3C-SiC. This shift can be explained by quantum – size effects at 3C-SiC/6H-SiC heteroboundary. Calculated position of first level in quantum well near 3C-SiC/6H-SiC heteroboundary (E0 =. 0,05 eV) is in good agrement with experimental value of EL shift. Finally we conclude, that by SEV it is possible to grow p– - 3C-SiC/n+ - 6H-SiC heterostructure with doping level in p- and n – regions suitable for investigation of 2DEG at heterobondary. This work was supported by the RFBR (grant N00-02-16688 and 01-02-17657) and NATO-SfP grant N978011.

K5.25
IMPLICATIONS OF GROWTH INDUCED DEFECTS ON THE ELECTRICAL AND MECHANICAL PROPERTIES OF AlN THIN FILMS ON SiC. Daniel Habersat, R.D. Vispute, S.S. Hullavarad, N. Reeves, B. Nagaraj, V.N. Kulkarni and T. Venkatesan, CSR, Department of Physics, University of Maryland, College Park, MD; C.J. Scozzie, Matt Ervin, and A. Lelis Army Research Laboratory, Adelphi, MD.

SiC possesses all the right properties such as wide band gap, high electrical breakdown strength and other unique properties to be used as a semiconductor in high power, high frequency and high temperature devices capable of operating in harsh environments. High temperature dielectrics on SiC are needed to overcome problems associated with thermal oxidation which results in excess of carbon leading to rough interfaces of SiC/SiO_2 with high density of interface traps and fixed charges. AlN with a dielectric constant of 8.5 that is very close to that of SiC eliminates the problem associated with high potential drop across the gate dielectric. We report on the effect of growth dependent mechanical and electrical characteristics of AlN thin films on 6H-SiC (0001) grown by pulsed laser deposition. AlN films were grown directly on silicon carbide (SiC) substrates at substrate temperatures ranging from room temperature to 1100°C. Films grown at 750-800°C were highly oriented while those grown at higher temperatures were epitaxial. However, the films grown at higher temperatures showed high interfacial stress and developed cracks along the crystallographic axes. Understandably, these films also showed high leakage currents. When AlN films were grown on a low temperature AlN buffer layer, the quality of AlN films greatly improved. In addition to the elimination of mechanical cracks in the dielectric films, substantial decrease in mean surface roughness, in-plane film stress and leakage currents have been observed. Effect of buffer layer on the evolution of epitaxial thin films with improved structural and electrical properties will be discussed.

K5.26
MECHANISTIC ASPECTS OF SiC OXIDATION. Fernanda Chiarello Stedile, Instituto de Química, UFRGS, Porto Alegre, BRAZIL; Cláudio Radtke, Israel Jacob Rabin Baumvol, Instituto de Física, UFRGS, Porto Alegre, BRAZIL; Ian Cameron Vickridge, Isabelle Trimaille, Jean-Jacques Ganem, Serge Rigo, Groupe de Physique des Solides, Université Paris, FRANCE.

SiC is the material of choice in the field of high band-gap semiconductors used in high-power, high-frequency, high-voltage, and/or high temperature applications. The possibility of obtaining an oxide film with good electrical characteristics (SiO_2) by thermal

oxidation is one of its major advantages. In order to develop an oxidation model, knowledge of the oxidation mechanism is of great importance. 6H-SiC(000$\bar{1}$) (carbon face) wafers were submitted to different oxidation processes in which the annealing time and O_2 gas pressure were varied. The incorporation of ^{18}O in surface and interface regions of the SiO_2 films were investigated performing first oxidations in natural ultra dry O_2 followed by oxidations using isotopically enriched oxygen ($^{18}O_2$). Different oxidation times in the natural gas were used to obtain samples representing different starting conditions to ^{18}O incorporation. ^{18}O contents and depth profiles were determined using nuclear reactions in plateau and resonance regions of their cross-section curves, respectively. The tracing results show an oxidation process limited by the interfacial reaction for SiC in our experimental conditions.

K5.27
OPTIMIZATION OF DIRECT N_2O GROWN GATE OXIDE ON 4H-SiC. K.Y. Cheong, and S. Dimitrijev, School of Microelectronic Engineering, Griffith University, Nathan Campus, Queensland, AUSTRALIA.

For silicon carbide (SiC) to fulfill its potential as an electronic material, methods must be developed to produce a high quality oxide and interface. Although it was shown that the quality of gate oxide directly grown in nitrous oxide (N_2O) is not as good as in nitric oxide (NO), N_2O is the preferred gas for used in industry due to its non-toxic property. In order for nitrogen (in N_2O) to contribute to interface passivation and to act as a carbon removal agent, the process parameters must be optimized. It was reported that the reliability of gate oxides directly grown in 10%-N_2O at 1175°C was better than for gate oxides grown in 100%-N_2O at 1100°C [1]. Recently, it was demonstrated by Lipkin et al. [2] that high temperature (1300°C) directly grown oxide in 100%-N_2O improved SiO_2-SiC interface quality and increased effective surface channel mobility. Given that this gas has a great potential for industry usage, the aim for this paper is to investigate the effects of N_2O concentration on the oxide and interface quality at high temperature (1300°C). Three sets of gate oxides were prepared by direct growth in different N_2O concentrations (100%, 10%, and 0.5%) at 1300°C on 4H-SiC. Among these samples, oxide growing in 10%-N_2O demonstrated the largest improvement in oxide and interface quality. Its electrical characterization showed the lowest interface trap and slow trap densities while atomic force microscopy revealed that the interface roughness was the smoothest. Also, nitrogen concentration characterized by x-ray photoemission spectroscopy (XPS) was the highest, and it was accumulated closest to the interface among these oxides. XPS also detected Si-$(OH)_x$ in bulk oxide for all samples, but 10%-N_2O grown oxide recorded the lowest atomic percentage. It is believed that this oxygen deficiency is the main contributor to the observed slow traps. References: 1. Jamet, P., Dimitrijev, S., and Tanner, P., J. Appl. Phys., 2001, 90, pp. 5058-5063. 2. Lipkin, L.A., Das, M.K., and Palmour, J.W., Tech. Dig. ICSCRM2001, Tsukuba, Japan, 2001, pp. 201-202.

K5.28
MONITORING ION IMPLANTATION OF SiC AND THE RECOVERY OF DAMAGE BY MICRO-RAMAN AND MICRO-PHOTOLUMINESCENCE SPECTROSCOPY. J.W. Steeds, S. Furkert, Department of Physics, University of Bristol, Bristol, UNITED KINGDOM.

Radiation damage caused by ion implantation causes loss of Raman scattering intensity so that the implanted areas can be mapped and profiled at a spatial resolution of 1μm. Subsequent annealing steps can be monitored by the recovery of the Raman signal and the appearance of damage-related photoluminescence peaks. These reveal broader profiles than those of the as-implanted regions on account of out-diffusion of damage during the annealing steps.

SESSION K6: SiC PROCESSING
Chairs: Stephen E. Saddow and Lisa M. Porter
Wednesday Morning, December 4, 2002
Room 206 (Hynes)

8:30 AM *K6.1
ALUMINUM AND BORON DIFFUSION IN 4H-SiC. Margareta Linnarsson, Martin Janson, Bengt Svensson, Royal Institute of Thechnology, Solid State Electronics, Stockholm, SWEDEN; Adolf Schöner, ACREO AB, Stockholm, SWEDEN.

Diffusion studies of dopant atoms in SiC date back to the 1960s. The main part of these investigations was performed by Vodakov and Mokov [1] utilizing autoradiography and pn-junction methods. Since the 1990s an increasing interest in dopant diffusions studies has emerged, strongly driven by an improved material quality and more demanding device applications. The boron diffusion coefficient in low-doped, n-type SiC (intrinsic conditions) is well established and an activation energy of 5.6 eV has been extracted. For ion-implanted n-type SiC, transient enhanced diffusion of both B and Al has been observed. The B diffusivity differs between n-type and p-type SiC and a Fermi-level dependence have been suggested. In the case of Al, literature data scatter somewhat between different experiment and no uniform picture can be revealed. In this contribution, the current status of aluminum and boron diffusion in SiC is discussed. Our recent results show a much higher mobility of boron in p-type compared to n-type 4H-SiC. For example, at 1400°C a boron diffusivity of 3×10^{-12} cm^2/s has been extracted in p-type 4H-SiC (3×10^{19} Al atoms/cm^3) which is almost three orders of magnitude higher than literature values for diffusion in low-doped, n-type SiC under intrinsic condition. A very strong dependence of the boron diffusivity on the aluminum concentration is revealed but our data do not favor a simple Fermi-level dependence. The mobility of boron is influenced by build in electrical fields where p-n junctions as well as gradients in the background dopant concentration affect the boron diffusion. For Al diffusion, a strong concentration dependence is observed. In low Al doped epitaxial SiC the Al mobility is negligible up to 2000°C but when the solubility limit is exceeded ($\sim2\times10^{20}$ cm^{-3}) a remarkable out-diffusion takes place already at ~1700°C. [1] E.N. Mokov et. al., Sov. Phys. Semicond. 18, 27 (1984).

9:00 AM K6.2
ELECTRICAL CHARACTERIZATION OF Al/Ti OHMIC CONTACTS ON P-TYPE ION IMPLANTED 4H AND 6H-SiC. Francesco Moscatelli, Andrea Scorzoni, Universita di Perugia, Dipartimento d'Ingegneria Elettronica e dell'Informazione, Perugia, ITALY; Antonella Poggi, Gian Carlo Cardinali, Roberta Nipoti, CNR-IMM Sezione di Bologna, ITALY; Mihai Lazar, Dominique Planson, Christophe Raynaud, Jean-Pierre Chante, Marie-Laure Locatelli, CEGELY (UMR CNRS n°5005), INSA de Lyon, Villeurbanne Cdx, FRANCE.

This paper deals with an electrical characterisation of low resistance ohmic contacts to p-type ion implanted 4H and 6H-SiC. Transmission Line Model (TLM) structures featuring two mask levels were fabricated by defining the doped strip below the contacts either by MESA etching of the implanted layer or by selective ion implantation. In all the cases the Al^+ species was implanted at different energies and fluence values so to produce box-shaped profiles. The implantation temperature, the plateaux concentration and the profile depth were 305°C, $4\times10^{19}cm^{-3}$ and 1.35 μm for the 6H-SiC wafer, and room temperature, $6\times10^{19}cm^{-3}$ and 0.5 μm for the 4H-SiC wafer. Both the samples were annealed at 1650°C for 30 min in Ar ambient. A metal scheme composed of Al(350 nm)/Ti(80nm) or Al(150 nm)/Ti(50nm) was deposited by sputtering, photolitography defined and annealed at 1000°C in Ar for 2 min. The average sheet resistance of the implanted layer, as computed both from TLM and Van der Pauw measurements, was 6700 Ω/square and 17000 Ω/square for the 6H-SiC and 4H-SiC wafers, respectively. The analysis of the TLM data by exploiting one-dimensional formulas gave an average contact resistivity equal to 4.5×10^{-4} Ωcm^2 and 1×10^{-3} Ωcm^2 for the 6H- and 4H-SiC sample, respectively. These formulas, however, are known to be valid only when the contact and doped region widths are identical, which was not the case with our structures. Using a 2-dimensional, finite difference simulation tool, the effect on the contact resistivity value due to the lateral current crowding in the doped area around the contacts was taken into account. In the case of the 6H-SiC wafer the 2-dimensional simulation showed that a contact resistivity value of the order of 2×10^{-4} Ωcm^2 accounted for the same experimental data. As expected, such a value is lower than that computed by the one-dimensional model. The simulation for the 4H-SiC TLM data is currently under way.

9:15 AM K6.3
OHMIC CONTACT PROPERTIES OF Ni/C FILMS ON 4H-SiC. Weijie Lu, Department of Physics, Fisk University, Nashville, TN; W.C. Mitchel, Air Force Research Laboratory, Materials and Manufacturing Directorate, Wright-Patterson Air Force Base, OH; J.R. Landis, University of Dayton Research Institute, Dayton, OH; T.R. Crenshaw, and W. Eugene Collins, Department of Physics, Fisk University, Nashville, TN.

The formation of high quality ohmic contact is a key issue in SiC device fabrications. Ni is the most common used metal for ohmic contact on n-type SiC. However, the mechanism of ohmic contact formation on SiC has not been understood. In this study, we present the ohmic contact formation of Ni/C film on n-type 4H-SiC and the effects of Ni catalytic graphitization. A graphitized carbon interfacial layer between Ni film and SiC can improve ohmic contact properties significantly. The thickness, annealing time, and annealing temperatures of Ni/C on SiC with various doping concentrations are examined. The optimal conditions for forming ohmic contact of Ni/C film on 4H-SiC with a doping concentration of 3.1×10^{19}cm^{-3} is to use a carbon interfacial film with a thickness of 2.0nm, and to be

annealed at 700-800°C in Ar for two hours, which results in a specific resistivity is at 10^{-6}-10^{-7} Ωcm^2. For the SiC with the doping concentrations of $1.6 \times 10^{18} cm^{-3}$ and $1.1 \times 10^{17} cm^{-3}$, the specific resistivities at 10^{-5} Ωcm^2 are measured after annealing at 900-1000°C in Ar for two hours. Raman spectroscopy, scanning electron microcopy (SEM), and atomic force microscopy (AFM) are used to characterize carbon structure evolutions and thin film morphology. The Raman spectra and morphological features on Ni/C/SiC can be interpreted by the well-known catalytic graphitization mechanism, e.g., the carbon diffusion and carbide decomposition process. Additional data of nine different metals with an interfacial carbon layer on SiC show that ohmic contact formation on SiC is determined by the catalytic graphitization activities of various metals. Nano-size graphitic flakes are responsible for ohmic contact formation on SiC, and metals as graphitization catalysts accelerate the formation of nano-size graphitic flakes.

9:30 AM K6.4
CONTROL OF MESA SIDEWALL ANGLE DURING THE INDUCTIVITY COUPLED PLASMA-REACTIVE ION ETCHING OF SiC SINGLE CRYSTALS. S.C. Ahn, B.T. Lee, Photonic and Electronic Thin Film Laboratory, Department of Materials Science and Engineering, Chonnam National University, Gwang-ju, KOREA.

In order to control mesa sidewall angle during the ICP-RIE and RIE etching of SiC single crystals, effects of etching gas (C2F6, NF3, SF6), mask material (Ni, SiO2, and PR), electrode material (stainless steel, anodized Al, alumina, SiO2) and gas addition (O2, CH4) on the etching characteristics were investigated At the "optimum" conditions, ICP-RIE of SiC using the C2F6, NF3, and SF6 plasma resulted in etch rate of about 100 nm/min, 400 nm/min and 300 nm/min, respectively. Vertical mesas with about 85° sidewall angle were obtained when the Ni etch mask was used. In the case of C2F6/O2 ICP-RIE, it was observed that the mesa angle decreased down to 70° when anodized Al or alumina was used as a electrode material, while this phenomenon was not observed in the cases of NF3 and SF6 plasma. In the case of NF3 and SF6 RIE, the sidewall angle could be reduced to about 30°and 60° by applying the PR mask and the SiO2 mask, respectively. The sidewall angle could be increased to 40°~60° by adding the CH4 gas to the plasma, in the case of PR mask and NF3 plasma were utilized. The mechanism responsible for these phenomena as well as results of detailed characterization will be also discussed in the presentation.

10:15 AM *K6.5
OPTICALLY ENHANCED INTERACTION OF HYDROGEN WITH DEFECTS IN SiC. Yaroslav Koshka, Dept of Electrical and Computer Engineering, Mississippi State University, Mississippi State, MS.

A new set of optical phenomena that could be observed only at low temperature in SiC was reported by the author's group during the past year. Dramatic changes in Al related photoluminescence (PL) were induced by high intensity optical excitation and occurred only in SiC epilayers contaminated with hydrogen. On the basis of the prediction of a broad diversity and complexity of recombination enhanced defect reactions in SiC made in an earlier study by P. J. Dean and W. J. Choyke [Advances in Physics, 26(1), 1-30 (1977)], the new phenomena were also attributed to carrier recombination or/and carrier trapping-stimulated processes. Later evidence suggested that the behavior of hydrogen in SiC under optical excitation is of a more general nature and is not limited to interaction with Al, which offered a model based on recombination enhanced athermal migration of hydrogen leading to a passivation of acceptor-related luminescence centers. In this work, a detailed review of the complexity of the non-reversible optically enhanced phenomena in 4H- and 6H-SiC will be given. New photoluminescence evidences will be suggested and supported by electrical measurements done on epilayers of different acceptor concentration. It will be established whether the changes in the PL spectrum stimulated by optical excitation are indeed a consequence of a modification of electrical activity of acceptors due to optically enhanced acceptor passivation or the observed phenomenon is a purely optical effect. The temperature dependence of the recombination-enhanced processes will be analyzed in the context of the available theoretical data on the charge states of hydrogen in SiC. Differences in efficiency of carrier capture by band-gap states at different temperatures will be also considered. A few alternative models for the observed temperature dependence will be presented and the most likely model will be identified depending on an outcome of currently conducted experiments.

10:45 AM *K6.6
POROUS SILICON CARBIDE: PROSPECTIVE APPLICATIONS. Marina Mynbaeva, Ioffe Physico-Technical Institute, St. Petersburg, RUSSIA.

Porous semiconductors have acquired a lot of attention centered on their specific properties as compared to the starting (bulk) semiconductor material. Porous materials, for example, have been an object of interest for use in various microelectronic devices such as photodiodes, light emitters, and gas sensors, and one of the modern approaches to improve the quality of homo- and heteroepitaxial semiconductor films is to use a substrate made of porous material. Recent developments in the technology of porous silicon carbide (PSC) for various applications will be reported on. First of all, we shall discuss the PSC fabrication technique, which allows one to fabricate porous SiC layers on the whole area of 2 inch 4H- and 6H-SiC substrates of various miscuts. PSC has been fabricated by surface anodization of commercially available n-SiC wafers. As-anodized wafers of both polytypes demonstrated mirror-like surface finish and morphology suitable for further epitaxial growth. The presence of PSC did not cause additional stress as related to the SiC substrate, as determined by micro-Raman spectroscopy. Anodized wafers were used as substrates for epitaxial growth to reduce the number of defects in the epitaxial SiC layers. Three epitaxial techniques were used, namely, sublimation growth, liquid phase epitaxy and chemical vapor deposition (CVD). The grown layers were analyzed from the point of view of surface quality, stress, and dislocation density. It was shown that of the three techniques used, CVD yielded the best layers. Following a detailed description of the use of porous layers as substrates for epitaxial growth, some new interesting properties of PSC, which have been discovered recently and must be considered when using porous material for practical applications, will be presented. Since the exact nature of PSC is still being studied, these new observations should accelerate the development of this material and its use in commercial devices.

11:15 AM K6.7
PSEUDOMORPHICALLY STRAINED LAYERS IN 4H SiC FORMED BY GERMANIUM IMPLANTATION. M.W. Dashiell, Xin Zhang, G. Xuan, and J. Kolodzey, Department of Electrical and Computer Engineering, University of Delaware, Newark, DE.

Low-energy ion implantation of germanium into 4H-SiC at 1273K resulted in crystalline SiC:Ge layers that are coherently strained to the (0001) oriented 4H-SiC substrates. Germanium implantation energies of 140keV and 50keV were chosen to form approximately 100nm thick step-like SiC:Ge layers with Ge atomic fractions ranging from 0.007 to 0.012. High-resolution x-ray diffraction (HRXRD) and reciprocal space mapping reveal a high quality, compressively strained SiC:Ge layer. The perpendicular x-ray strain of the as-implanted region ranges from 0.0008 to 0.015 depending on the dose. High-temperature annealing resulted in partial relaxation of the macroscopic layer strain, however the SiC:Ge layer remained pseudomorphic for annealing up to at least 1873 K. Strong Pendellsung fringes in the HRXRD spectra indicate coherent strain and the absence of dislocations before and after annealing. Because Ge is a group-IV atom like Si and C, its substitutional incorporation into the lattice is expected to act as an isoelectronic impurity, rather than a charged donor. Thus, high-quality, pseudopmorphic-strained SiC:Ge layers have potential for bandgap and strain engineered electronics such as SiC-based high electron mobility transistors (HEMTs) for RF-power electronics. Currently there is no established heterojunction pair in SiC material technology for fabricating HEMTs and other heterojunction devices.

11:30 AM K6.8
BAND LINE-UP OF 4H-SiC SCHOTTKY INTERFACES MEASURED WITH PHOTOEMISSION SPECTROSCOPY. M. Beerbom, J. Kohlscheen, S.E. Saddow, J.T. Wolan, University of South Florida; G. Chung, M.F. MacMillan, Sterling Semiconductor, Inc.; and R. Schlaf, University of South Florida.

4H-SiC/metal interfaces were investigated using photoemission spectroscopy. The interfaces were prepared by depositing Ni and Al on p- and n-doped 4H-SiC substrates. The metal films were grown in several steps starting at sub-monolayer coverages. In between deposition steps photoemission spectroscopy measurements were carried out yielding thickness dependent series of spectra. These spectra give detailed information about the chemical structure of the interface as well as the band line-up at the metal/semiconductor boundary. The investigation of p- and n-type interfaces allowed to distinguish between chemical reaction related peak shifts and shifts originating from the development of band bending. Evaluation of the band bending related core level peak shifts in conjunction with the valence band maximum position enabled the determination of the hole injection barriers at the interfaces. The corresponding electron injection barriers were determined by incorporation of the optical band gap of SiC.

SESSION K7: DEVICES
Chairs: Gerhard Pensl and Roland Rupp
Wednesday Afternoon, December 4, 2002
Room 206 (Hynes)

1:30 PM *K7.1
SYSTEM DESIGN CONSIDERATIONS FOR OPTIMIZING THE BENEFIT BY UNIPOLAR SiC POWER DEVICES. Roland Rupp, Ilia Zverev, Infineon Technologies AG, Dep. AI PS, Erlangen, GERMANY.

Close-to-ideal properties of silicon carbide unipolar devices are superlative for hard switching commutation. In order to maximize the benefit from these characteristics different design trade off's are required compared to conventional unipolar devices. Example 1: Active Power Factor Correction (PFC): Boost converters are usually used to realize active power factor correction. SiC diodes have a limited inrush surge current capability. The initial charge of a bulk capacitor during the plugging in can exceed the maximum allowed peak current through the booster diode. This can be avoided using a bigger die size SiC diode (causing impact on cost) or using a conventional silicon diode in parallel for bypassing. During start up the Control IC will try to charge the bulk cap as fast as possible. This leads to very long duty cycles for the diode. Combination of high peak current and long duty cycles causes large conduction power losses in the diode. Bigger SiC die's (impact on cost) or some soft starting technique's solve the problem. Selecting the current rating for the PFC boost diode is an important design consideration. Differently rated currents mean different die sizes, power losses and cost. An optimal solu-tion would be obviously the smallest die size, which can handle defined output power under given thermal considerations in steady state. Diode's leakage current can be increased due to application conditions in order to optimize forward characteristic. Using SiC Schottky diodes the total power losses in the PFC system (including switch, choke and bulk capacitor) have a minimum at a reasonable switching frequency. The PFC system can be optimized for highest efficiency or highest power density (size). Example 2: Switch Mode Power Supply (SMPS): The properties of SiC JFETs like higher blocking voltages then Si MOSFET combined with higher switching speed allow completely new directions in SMPS system design.

2:00 PM *K7.2
PiN RECTIFIERS AND BIPOLAR SWITCHES IN 4H-SiC. Ranbir Singh, D.C. Capell, J.J. Sumakeris, and St. G. Müller. Cree Inc., Durham, NC.

SiC is a superior material system for the fabrication of ultra high voltage devices since it is capable of sustaining a high power density, which can be switched at an extremely high speed, while operating at high temperatures. Such devices would be suitable for solid state power conditioning systems for high power radar, directed energy weapons, X-ray generators, electrostatic precipitators and high power LASERs. This paper describes the development of high power rectifiers and bipolar switches in the recent past. Some experiments to understand the forward voltage drift issue are also explained. In the past 5 years, PiN rectifier voltage ratings have increased from 2.2 kV up to 19 kV. On some 7.4 kV rectifiers, a pulsed current of 330 A have been measured. These increases have been directly attributed to an increase in the material quality as well as a better understanding of basic design and processing issues related to these devices. The most successful design to date for high power PiN rectifiers has been a mesa-JTE structure. These diodes utilizes a high purity, extremely thick n- epitaxial layer doped layer grown using a refined hot wall CVD growth reactor yielding low epi defect densities. On these voltage blocking layer, a highly doped, p+ Anode was grown epitaxially in order to obtain good carrier injection during on-state operation. To prevent premature breakdown, the voltage-blocking layer was exposed using reactive ion etching, and a wide, optimized Junction Termination Extension (JTE) is implemented using a p-type implant at the periphery of the device edge. The SiC surface at the edges are then passivated using a thick SiO2 layer. Recently, a peculiar problem has been identified to challenge the use of these high performance rectifiers in widespread use. Due to the very low stacking fault energy of SiC, stacking faults may nucleate from specific pre-existing defects in SiC bipolar device structures and grow under typical forward conduction conditions. Extensive growth of these defects can attenuate the electron-hole plasma present in the device during forward operation and lead to an increase in the forward voltage of the overall device structure. Degradation of the forward voltage is a significant barrier to fully exploiting the capabilities of SiC bipolar devices, especially in applications that employ several devices in parallel for current sharing. We have studied the formation and growth of stacking faults in test PiN diodes with both solid and windowed topside ohmic contacts to permit direct observation of stacking faults in diodes via electroluminescence. We have characterized specific types of test diodes in terms of stacking fault density and extension. In addition, EBIC imaging has been used to study the faults and forward voltage drift measurements have been conducted to track the change in forward voltage during extended operation. Maintaining a stable forward voltage for bipolar SiC devices, as with all high quality device fabrication, requires maintaining the integrity of the material all the way from the growth of the boule to device packaging and operation. In one aspect of our research, we have identified and applied specific techniques of epilayer growth and device fabrication to stabilize the forward voltage of test PiN diodes produced on commercially available 4H-SiC wafers. These techniques have enabled the fabrication of simple devices that do not exhibit significant forward voltage drift under 300A/cm2 stress for 40 hours. While our research has determined that the effect of any specific process change must be evaluated in the context of a complete device fabrication methodology, several critical device-processing areas that will require additional scrutiny will be identified for discussion.

2:30 PM K7.3
SiC BIPOLAR JUNCTION TRANSISTORS FOR HIGH POWER SWITCHING AND RF APPLICATIONS. Anant Agarwal, Sei-Hyung Ryu, John Palmour, Cree Inc., Durham, NC; Binh Phan, Howard Bartlow, Jerry Stambaugh, Ken Brewer, Cree Microwave, Sunnyvale, CA.

Silicon Carbide (SiC) is a very attractive material for high voltage, high power RF devices. Power MOSFETs in SiC have received much of the attention, but these have shortcomings due to poor MOS mobility and reliability, especially in 4H-SiC. On the other hand, bipolar devices such as GTO's have demonstrated high blocking voltages and high on-currents, taking full advantage of the material properties of SiC. In this paper, high performance, high voltage NPN bipolar junction transistors in 4H-SiC are presented for applications in low frequency (< 5 MHz) power conversion systems as well as in RF (425 MHz) power amplifiers. To date, both epitaxial and implanted emitter 4H-SiC bipolar junction transistors (BJTs) have been demonstrated. It has been found that the epitaxial emitter results in a higher current gain than the implanted emitter structure due to the implant induced damage in the base and emitter regions in the latter structure. The power BJTs for low frequency switching applications were able to block 1200-1800V and showed an on-resistance of <10 mohm-cm^2, which outperforms all SiC power switching devices ever reported. Moreover, these transistors show a positive temperature coefficient in the on-resistance characteristics, which enables easy paralleling of the devices. The RF BJTs had a maximum current gain of about 15. The common emitter breakdown voltage was in excess of 500 V consistent with the 5 micron collector thickness. The fT of the cell was measured under large signal conditions as a function of the collector current with different collector supply voltages. For VCC = 20 V, fT peaked at about 1.5 GHz. A single cell was measured in common emitter mode with a collector supply voltage of 80 V in class AB at 425 MHz. A 100 micro-second pulse width with 10% duty cycle was used. A maximum output power of 50 W for a single cell is achieved. This represents an output power density of 47 kW/cm^2 when normalized by the active base area. The peak large signal power gain was 9.6 dB. The collector efficiency at the power output of 50 W was 51% with a power gain of 9.3 dB. This represents the first demonstration of a SiC RF BJT.

2:45 PM K7.4
ELECTRICAL INSTABILITY SUPPRESSION IN 4H-SiC POWER MESFETs. J.B. Tucker[a], R.A. Beaupre[a], A.P. Zhang[a], J.L. Garrett[a], A. Vertiatchikh[a], L.B. Rowland[a], E. B. Kaminsky[a], J.W. Kretchmer[a], J. Foppes[b], A.F. Allen[b], L.F. Eastman[c]; [a]General Electric, Global Research Center, Niskayuna, NY; [b]LM NE&SS-Radar Systems, Syracuse, NY; [c]Cornell University, Ithaca, NY.

SiC has attracted great interest for high power microwave applications because of its superior intrinsic properties in comparison to Si and GaAs. Steady demonstration of high power handling capability has been achieved in recent years. However, SiC MESFETs still suffer from significant drain current degradation under RF operation or long-term DC stress. This degradation can be recovered by illumination under UV light. The origin of this effect has been attributed to either trapping at the device surface between the source and drain or trapping at the epi-substrate interface due to the presence of Vanadium in the bulk. Newly available high purity (non-Vanadium compensated) bulk SiC substrates were used in an effort to limit the effect of Vanadium-related deep level trapping. To investigate the effect of Vanadium on SiC MESFET performance, we compare similar devices fabricated on conductive, semi-insulating (Vanadium compensated), and semi-insulating (high-purity) 4H-SiC substrates. Pulsed I-V measurements as well as current- and capacitance-based deep level transient spectroscopy (DLTS) measurements were performed to assess trapping activation energy, physical location, and density. An assessment of device performance and reliability for each substrate type is made using RF load-pull measurements and device long-term DC stressing. Device RF load-pull power, small signal ft, fmax, and Idss are also reported.

3:15 PM *K7.5
INFLUENCE OF INTERFACE STATES ON HIGH TEMPERATURE SILICON CARBIDE ELECTRONICS AND SENSORS. Ruby N. Ghosh, Peter Tobias, Sally G. Ejakov and Brage

Golding, Center for Sensor Materials, Michigan State University, East Lansing, MI.

Silicon carbide based metal-oxide-semiconductor (MOS) devices are well suited for operation in chemically reactive high temperature ambients. Applications include control and feedback electronics for electricity producing turbines as well as gas sensors for monitoring automotive and power plant emissions such as hydrocarbons. The response of catalytic gate SiC MOS sensors (such as $Pt/SiO_2/SiC$ capacitors) to hydrogen-containing species has been assumed to be due to the formation of a dipole layer at the metal/oxide interface, which gives rise to a voltage translation of the high frequency capacitance voltage (C-V) curve. We have discovered that high temperature (800 K) exposure to hydrogen results in (i) a flat band voltage occurring at a more negative bias than in oxygen and (ii) the transition from accumulation to inversion occurring over a relatively narrow voltage range. In oxygen, this transition is broadened indicating the creation of a large number of interface states. We interpret these results as arising from two independent phenomena a chemically induced shift in the metal/semiconductor work function difference and the passivation/creation of charged states (D_{IT}) at the SiO_2/SiC interface Our results are important for both chemical sensing and electronic applications. From in-situ C-V spectroscopy, performed in a controlled gaseous environment to 900 K, we have determined that hydrogen exposure results in a near ideal interface whereas oxygen exposure creates interface states. The interface state density is energy dependent, small around mid-gap and increases towards the conduction band. MOS capacitance gas sensors typically operate in constant capacitance mode. Since the slope of the C-V curve changes dramatically with gas exposure, we discuss how sensor reliability and response time are influenced by the choice of operating point. For electronic applications understanding the environmentally induced changes in D_{IT} is crucial to designing drift-free MOS devices.

3:45 PM *K7.6
TOWARDS FERROELECTRIC FIELD EFFECT TRANSISTORS IN 4H-SILICON CARBIDE. S.-M. Koo, S.I. Khartsev, C.-M. Zetterling, A.M. Grishin, and M. Ostling, Department of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Stockholm-Kista, SWEDEN.

So far, metal-ferroelectric-(insulator)-semiconductor structures on wide-bandgap semiconductors have been examined for their stability at temperatures over 900°C, as well as for their superior materials properties for various device applications. Silicon carbide (SiC), being the only wide-bandgap material of which bulk wafers are currently available, is promising for high power, high temperature, and high frequency applications. Recently we have reported properties of PZT/Al_2O_3/4H-SiC diode structures (Appl. Phys. Lett., **81**, July 2002): stable capacitance-voltage $C-V$ loops with low conductance ($< 0.1\ mS/cm^2$, $\tan\delta \sim 0.0007$ at $400kHz$) and memory window as wide as $10V$ were obtained when $5nm$-thick Al_2O_3 was used as a high bandgap ($E_g \sim 9eV$) barrier buffer layer between PZT ($E_g \sim 3.5eV$) and SiC ($E_g \sim 3.2eV$). PZT/Al_2O_3 gate stacks enable superior $C-V$ characteristics with negligible sweep rate dependence and saturation at low bias voltages compared to PZT directly deposited on SiC. PZT/Al_2O_3/SiC gate stack looks very promising for non-volatile memory and SiC-based high-frequency and high-temperature device applications. Based on this structure, different types of the metal-ferroelectric-silicon carbide FETs have been designed to operate in depletion or enhancement mode operations. Further experiments for the characterization of non-volatile performance and improved channel mobility in prototype devices are in progress and the results will be presented.

4:15 PM K7.7
7 kV 4H-SiC GTO THYRISTORS. Stephen Van Campen, John Zingaro, Andris Ezis, Garrett Storaska, Kevin Elliott, R. Chris Clarke, Northrop Grumman, Advanced Materials and Semiconductor Device Technology Center, Baltimore, MD; Vic Temple, Todd Hansen, Silicon Power Corporation, Malvern, PA.

High power asymmetric SiC GTOs (Gate Turn-Off Thyristors) were fabricated on n-type 4H-SiC substrates and tested to investigate breakdown voltage, maximum current density, switching characteristics, and temperature dependences. Comparison between Guard Ring edge termination and a proprietary Junction Termination Extension (JTE) fabricated on the same wafer, reveal that the JTE outperforms the Guard Rings when comparing breakdown voltages. GTOs with active areas of 0.5 mm^2 and 4 mm^2 were fabricated using a mesa-etch process. A device structure consisting of five epitaxial layers was used to form the active regions of the GTO. The drift layer is a 50 μm thick, p-type epi, doped between $2-8 \times 10^{14}$ cm^{-3} for an individual wafer. The device surface is passivated with a thick layer of oxide. Individual 4 mm^2 GTOs utilizing the JTE were tested in forward bias and found to support over 5 kV at leakage currents of less than 5 μA. In addition, smaller area GTOs (0.5 mm^2) utilizing the JTE were found to support over 7 kV. These blocking voltages are the highest reported for switching devices in SiC. The on-state characteristics are equally impressive, with the large devices carrying 20 A. The GTO has a forward voltage drop of 4 V at a current density of 100 A/cm^2 and a differential on-resistance of 10 $m\Omega$-cm^2. This indicates that on-state losses should not be excessive even at high current density. Switching losses are another important characteristic of power GTOs. Gate turn-on and turn-off gains were measured to investigate switching efficiency and power dissipation.

4:30 PM K7.8
FABRICATION AND CHARACTERIZATION OF 4H-SILICON CARBIDE AVALANCHE PHOTODIODES. Kent Burr, Peter Sandvik, Stephen Arthur, Dale Brown, Kevin Matocha, GE Global Research Center, Niskayuna, NY.

Avalanche photodiodes (APDs) that are sensitive in the UV from approximately 250 350 nm have been fabricated from 4H-Silicon Carbide. The SiC APDs, which use hole-initiated avalanche multiplication, were produced using n-type SiC epitaxial layers grown on a p-type substrate. In order to achieve avalanche breakdown in the bulk of the material, a dry ion-based etching technique was used to form sloped sidewalls on the devices. The devices had an area of approximately .1 mm^2, and they had maximum breakdown voltages of approximately 500 V. The APDs had a positive temperature coefficient for avalanche breakdown voltage and showed excellent stability for multiplication factors in excess of several hundred. Dark current, photo responsivity, and multiplication measurements from room temperature to 150°C will be presented. The dark noise performance of the APDs has also been characterized using a standard nuclear spectroscopy system consisting of a charge sensitive preamplifier, a shaping amplifier, and a multichannel analyzer. The input equivalent dark noise charge and excess noise factor for the dark current was measured over a range of shaping times, temperatures, and bias voltages. The noise performance of SiC APDs in applications such as gamma ray or x-ray spectroscopy will be highly dependent on the achievement of low bulk leakage current at the operating point.

4:45 PM K7.9
A NEW PROCESS FOR THE FABRICATION OF SCHOTTKY DIODES AND MESFETS ON SiCOI (SILICON CARBIDE ON INSULATOR) SUBSTRATES. Francois Templier, CEA-LETI, Grenoble, FRANCE; Nicolas Daval, SOITEC, Bernin, FRANCE and CEGELY-INSA, Villeurbanne, FRANCE; Fabrice Letertre, SOITEC, Bernin, FRANCE; Daniel Bourgeat, CEA-LETI, Grenoble, FRANCE; Dominique Planson and Jean-Pierre Chante, CEGELY-INSA, Villeurbanne, FRANCE; Thierry Billon, CEA-LETI, Grenoble, FRANCE.

The Schottky diode has been the first silicon carbide device to come on the market, with outstanding switching characteristics combined with high ON current. However, the small size, high cost of SiC substrates are still disadvantages which limit fast expansion of such devices. SiCOI material (Silicon Carbide On Insulator) is a very promising low cost substrate, providing 4, 6 or 8 inches wafer sizes which are silicon-line compatible. The main characteristic of the SiCOI structure is the buried oxide between the SiC active layer and the handle substrate. This layer prohibits vertical conduction, which imposes to design horizontal device, but provides the integration of devices, thanks to galvanic insulation. Those points speak for a promising substrate in the fields of power systems on single chip, low-cost and easy-processing SiC substrates. This article will present for the first time the design, development and fabrication of power SiC Schottky diodes on 4 inches SiCOI substrates. Targeting a 600V / 1 Amp Schottky diode, we performed electro-thermal simulations, and designed a lateral device. The doping level of the active layer was 2×10^{17} cm^{-3} and its thickness 0.5 μm. The edge termination is obtained by an original slopped Schottky contact combined with field plate. We have developed a process to fabricate the Schottky diodes on the 4 inches SiCOI substrates. The main challenge was the realization of the slopped Schottky contact. The process also provides the fabrication of SiC MESFETs, on the same wafer, without additional step. These SiC devices were fully processed on a 4 inches silicon line, including lithography using automated resist coating line and exposure tool. Fabrication process will be presented and discussed, as well as electrical results.